Master–Thesis

Development and Test of a Universal FPGA–based Arc Detector for Accelerating Cavities at the Facility for Antiproton and Ion Research FAIR

Mathieu Omet

Technische Universität Darmstadt
GSI Helmholtzzentrum für Schwerionenforschung GmbH

First reviewer:	Prof. Dr. Joachim Enders
Second reviewer:	Dr. Ulrich Laier
Supervisor:	Dipl.–Ing. (FH) Stefan Schäfer
Day of submission:	5th of August 2011

Abstract

In this work, the design, the actual realization and the test of a detector for electric arcs in accelerating cavities is described.
After the assessment of several methods detecting an electrical arc, a digital solution has been chosen, which is based on the comparison between the ratio of the amplitudes of actual values of the control grid voltage of the tetrode and the gap voltage of the respective cavity and a preset threshold. In order to realize the arc detector, hardware that was developed by the radio frequency group at GSI Helmholtzzentrum für Schwerionenforschung GmbH was used. The implementation of the algorithm was made with the programming language VHDL on a Cyclone III field programmable gate array from Altera.
After a reconfiguration of the hardware according to the requirements has been made, a multipurpose detector framework, which allows a convenient realization of diverse types of configurable detectors, was developed and implemented. In order to realize the arc detector the arc detector core was developed and implemented within the detector framework. The user–friendly configurability via PC, especially of the threshold of the trigger condition as well as of the offset and scaling adjustment of the input signals, was included. The functionality of the arc detector was extended by that of an amplitude detector so that beside the digital trigger signal also the amplitudes of the input signals are available as analog output signals.
The functionality of the arc detector has been verified within a test setup. It was shown that all requirements have been fulfilled without any exception. The trigger response time is 7.8 $\pm$ 0.1 μs . The amplitude response time for amplitude–to–digital converter–channel 1 is 12.9 $\pm$ 0.1 μs and 12.6 $\pm$ 0.1 μs for amplitude–to–digital converter–channel 2. The dynamic range for channel 1 is 47.3 $\pm$ 0.1 dB and 36.4 $\pm$ 0.1 dB for channel 2. The frequency dependency of both amplitude output signals is 6%.
This made it justifiable to test the arc detector in a test cavity that is similar to the cavities used in heavy–ion synchrotron SIS 18, which yielded a partly confirmation of application. In case of realistic acceleration cycles using frequency and amplitude ramps glitches on the trigger signal of the arc detector occurred. These originate from a timing problem in the algorithm caused by an insufficient synthesis due to a complex and extensive routing during the fitting process because of the consumption of over 75 % of the resources of the field programmable gate array.

Zusammenfassung

In der vorliegenden Arbeit wird die Entwicklung, der Aufbau und der Test einer Überschlagserkennung für Kavitäten beschrieben.
Nach dem Abwägen verschiedener Methoden zur Detektion von Überschlägen wurde sich für eine digitale Lösung entschieden, die auf dem Vergleich des Verhältnises von Amplituden der Steuergitterspannung der Tetrode und der Gapspannung der entprechenden Kavität mit einem vorgewählten Schwellwert basiert. Um den Überschlagsdetektor zu realisieren, wurde auf Hardware zurückgegrifen, die in der Ring–Hochfrequenz–Arbeitsgruppe an der GSI Helmholtzzentrum für Schwerionenforschung GmbH entwickelt wurde. Die Implementierung des Detektors geschieht mit Hilfe der Programmiersprache VHDL auf einem Field Programmable Gate Array der Firma Altera.
Nach der Rekonfiguration der Hardware entsprechend den Anforderungen wurde ein universal verwendbares Detector–Framework, das eine einfache Realisierung verschiedenster konfigurierbarer Detektortypen ermöglicht, entwickelt und implementiert. Um den Überschlagsdetektor zu realisieren, wurde der Arc–Detektor–Core entwickelt und in das Detector–Framework eingebunden. Dabei wurde auch eine benutzerfreundliche Konfigurierbarkeit per PC insbesondere des Schwellwertes der Triggerbedingung wie auch des Offsets und der Skalierung der Eingangssignale berücksichtigt. Die Funktionalität des Überschlagdetektors wurde um die eines Amplitudendetektors erweitert, so dass neben dem digitalen Triggersignal auch die Amplituden der Eingangssignale als analoge Ausgangssignale zur Verfügung stehen.
Die Funktionalität des Überschlagdetektors wurde in einem Testaufbau verifiziert. Es konnte gezeigt werden, dass alle Anforderungen ohne Ausnahme erfüllt wurden. Die Asprechzeit des Triggers liegt bei 7,8 $\pm$ 0,1 μs, die Anstiegszeiten für die Amplitudendetektion bei 12,9 $\pm$ 0,1 μs für den Analog–to–Digital Converter–Kanal 1 und 12,6 $\pm$ 0,1 μs für den Analog–to–Digital Converter–Kanal 2. Dabei weist Kanal 1 einen Dynamikbereich von 47,3 $\pm$ 0,1 dB und Kanal 2 von 36,4 $\pm$ 0,1 dB auf. Der Frequenzgang beider Amplitudenausgänge liegt bei 6%.
Dies rechtfertigte einen Testlauf des Detektors in der SIS–18–Testkavität, die der am Schwerionen–Synchrotron SIS 18 gleicht, bei dem dessen Funktionalität teilweise bestätigt wurde. Im Falle von realistischen Beschleunigungszyklen mit Frequenz- und Amplitudenrampen traten Störsignale auf, die zu einer Fehltriggerung führten. Diese Störsignale werden durch ein Timingproblem im Detektionsalgorithmus verursacht, das darauf zurückzuführen ist, dass die Synthese wegen der Ausnutzung von über 75 % der Resourcen des Field Programmable Gate Arrays und dem dadurch kompexen und aufwändigen Routing während des Fittenvorgangs unzureichend ist.

Contents

Chapter 1

Introduction

1.1 Particle Accelerators

In order to produce beams consisting of charged particles, particle accelerators are needed. In this chapter electrostatic and radio–frequency accelerators are introduced. Detailed information is provided elsewhere [1, 2].

1.1.1 Electrostatic Accelerators

- **Cathode Ray Tube**

The most common electrostatic particle accelerator is the cathode ray tube that was invented by Karl Ferdinand Braun in 1879. Electrons that are emitted by a cathode are accelerated towards an anode due to an electric potential. The particles are bundled to a beam by a static magnetic field produced by focusing coils. The direction of the beam can be defined by a variable magnetic field caused by deflection coils. A major field of application using this principle were cathode ray tube screens. According to present convention the cathode ray tube is not called a particle accelerator. This term is reserved for devices achieving particle energies of more than 1 MeV.

- **Cockroft–Walton Accelerator**

The Cockroft–Walton accelerator was invented by Cockroft and Walton in 1932. Its principle is based on the conversion of low level AC (Alternating Current) voltage to a higher DC (Direct Current) voltage. Therefore a voltage multiplier ladder network of diodes and capacitors is used. This kind of accelerators is still used for preacceleration. It achieves particle energies of up to 750 kV.

- **Van de Graaff Accelerator**

The Van de Graaff accelerator was invented by Robert Jemison Van de Graff in 1930. The voltage for the acceleration is generated by using a continuously moving non conductive belt between two pulleys. At the lower pulley positive charge is attached to the up moving part of the belt. This charge is removed from the belt at the upper pulley and transfered to a high–voltage terminal. This way an electric potential between the high–voltage terminal and the ground is created. Van de Graaff accelerators are also used as preaccelerators and achieve particle energies up to 25 MV.

- **Tandem Accelerator**

The principle of a tandem accelerator is the same as the of a Van de Graaff accelerator, despite that the electric potential is used twice. This is realized by accelerating negative charged particles. In a second step the electrons of this particles are stripped by a thin foil in order to alter the charge to positive. This way the same electric potential can be used a second time. Particle energies up to 40 MV can be achieved.

1.1.2 Radio–Frequency Accelerators

- **Wideroe Linear Accelerator**

The Wideroe linear accelerator (linac) was the first radio frequency accelerator. A time–alternating voltage is applied to a sequence of tubes in such a way that the particles are always at the right time at every gap to be accelerated. Thus the length of the tubes is increasing respectively to the velocity of the particles. During the phase that would decelerate the particles, they are shielded by the tubes. Figure 1.1 shows a principle of the accelerator [2].

Due to the fact that linear accelerators for high particle energies are respectively long, it is desired to keep the particles on a circular path.

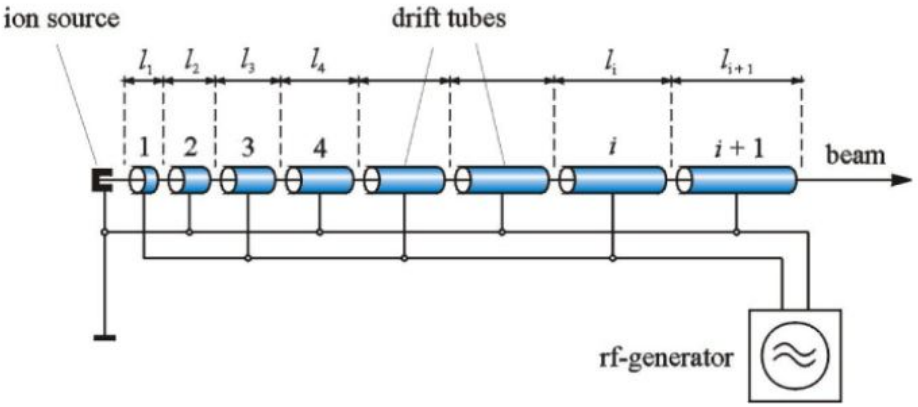

Figure 1.1: *Principle of the Wideroe linear accelerator. On the left hand side particles are emitted by an ion source. RF voltage is applied to the drift tubes, which have an increasing length. The particles are accelerated towards the right hand side.*

- **Cyclotron**

In a cyclotron the particles are emitted near the center of two D-shaped metal chambers and are deflected by a homogeneous magnetic field. The particles are accelerated at the gap of the two electrode chambers due to an oscillating electric field. The combination of deflection and acceleration let the particle move on a helix path. Figure 1.2 shows a principle of a cyclotron [2].

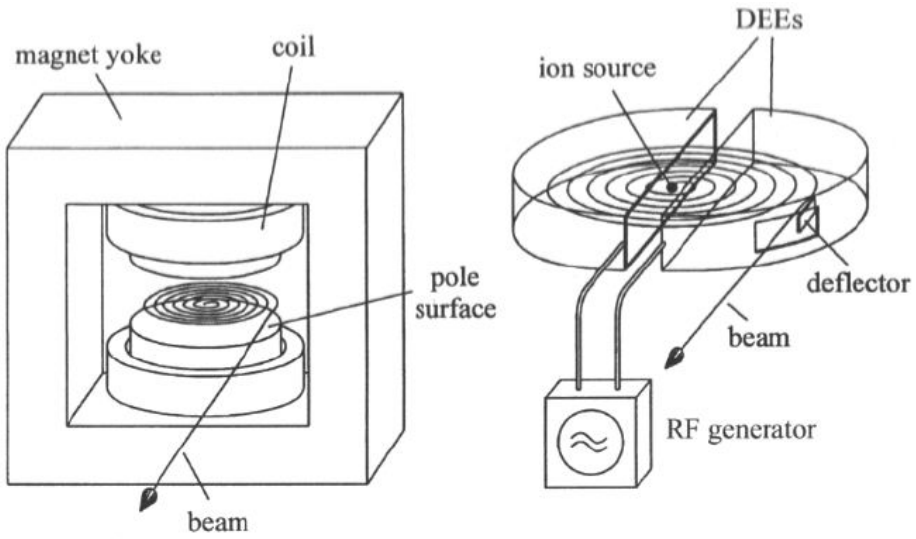

Figure 1.2: *Principle of the cyclotron: On the left hand side a principle of the outer part of the cyclotron shown including the magnet yoke and the coil, which are used for producing a homogeneous magnetic field. On the right hand side there are two D-shaped metal chambers that are connected to a RF generator. Near the center of the chambers the ion source is located. The right chamber has got an deflector for extracting the beam.*

- **Synchrotron**

The synchrotron is a cyclic particle accelerator in which the particles move on a circular orbit. It consists mainly of pipes for beam transportation, cavities for acceleration of the particles, dipole magnets for bending the particle beam, and quadrupole magnets for focusing the beam. In order to transfer the beam into or out the synchrotron kicker magnets are used. In the whole accelerator a vacuum is produced in order to minimize collisions of the beam with gas molecules. Due to the fact that magnetic and electric fields of the dipole magnets and acceleration cavities are ramped synchronously the accelerator is called synchrotron. Figure 1.3 shows the heavy–ion synchrotron SIS–18 at GSI [3] as an example.

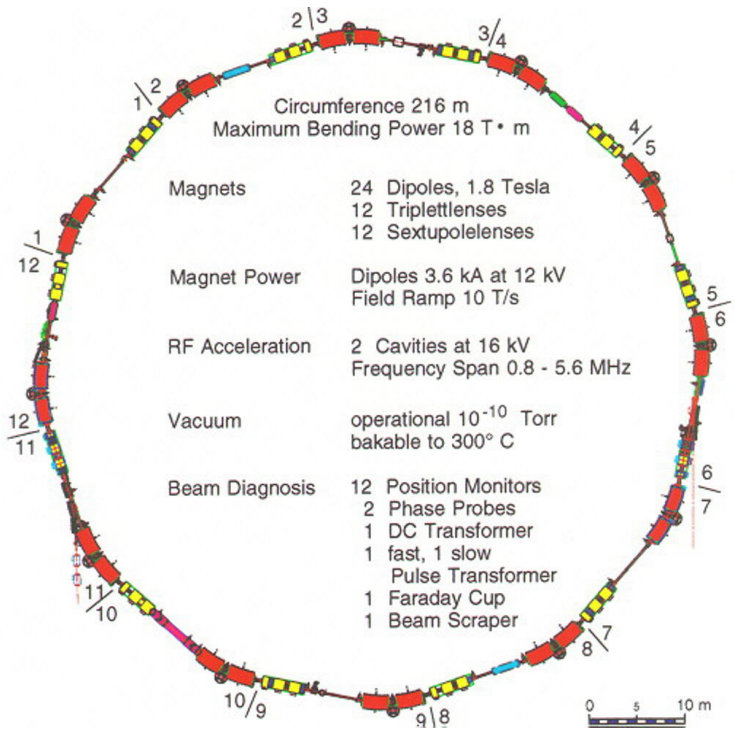

Figure 1.3: *Schematic of heavy–ion synchrotron SIS–18. The dipole bending magnets are illustrated in red, the quadrupole focusing magnets in yellow, and the acceleration cavities in blue. The SIS–18 is divided in twelve similar cells.*

1.2 Radio–Frequency Acceleration

In this chapter the base item of longitudinal dynamics of the radio–frequency acceleration is introduced. Detailed information about this topic is provided elsewhere [1, 2].

In order to accelerate charged particles to high energies electromagnetic RF waves produced in cavities are used. The particles passing the cavities that are synchronous to the phase of the RF wave are called synchronous particles. The energy gain of such particles is

$$\Delta W = qV_0 \cos \Phi_s \quad , \tag{1.1}$$

where q is the charge of the particle, V_0 the voltage amplitude, and Φ_s the phase of the RF wave. For a detailed derivation see section 1.3.1. The

energy of a synchronous particle is

$$W_s = m_0 \gamma c^2 \quad , \tag{1.2}$$

where m_0 is the rest mass of the particle, $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ with $\beta = \frac{v}{c}$, and c the speed of light.
In an accelerator using RF acceleration like for e.g. a synchrotron the particle beam is bunched. The area of the phase space of the particles in which the bunch is located is called bucket. The bucket is separated by the separatix (cf. figure 1.4) from the rest of the phase space in which particles on divergent path are located. Due to the distribution of the particles in the bunch the majority will not be at the location of the ideal particle. In order to accelerate the whole bunch a phase of the RF wave is chosen in such way that the ideal particle arrives as near as possible to the maximum of the rising edge while leaving enough space for the rest of the bunch. Thus the bunch is trapped at a potential minimum in which the particles oscillate. The frequency for this oscillation is called synchrotron frequency

$$\omega_s = \sqrt{-\frac{2\pi q V \sin \Phi_s}{\beta^2 \gamma^3 \lambda_{RF}^2 m}} \quad , \tag{1.3}$$

where λ_{RF} is the wavelength of the RF wave. In phase space this oscillation causes a movement on closed orbit of the particles. Figure 1.4 shows a plot of the RF wave, the RF potential, and the trajectories of the particles in phase space [3].

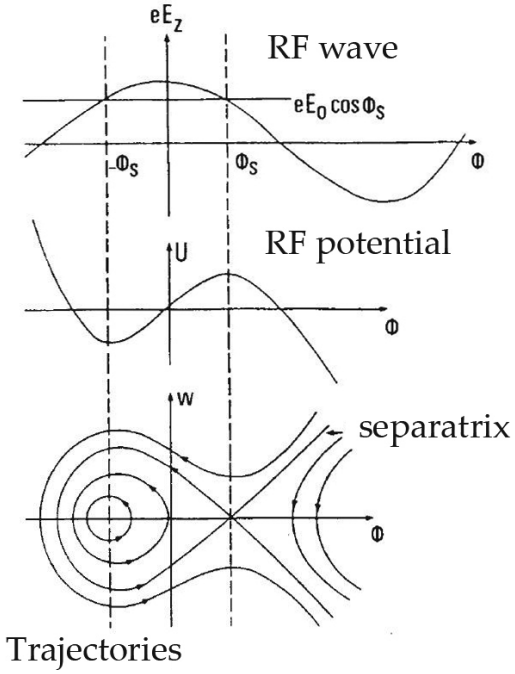

Figure 1.4: *Particle Dynamics in an RF Field: On the top the z component of the electric field of the RF wave is plotted as a function of phase. In the middle the RF potential is plotted as a function of phase. At the bottom the phase space with particle energy as a function of phase is plotted. In all three plots the location of the ideal particle is marked with the left dashed line.*

1.3 Acceleration Cavities

1.3.1 Types of Cavities

- **Pillbox Cavities**

A pillbox cavity is a hollow structure in which an electromagnetic mode can be excited in order to accelerate particles. To achieve high energies in linear accelerator a particle has to pass a sequence of cavities. In a circular accelerator usually one or more cavities are used through which the particles pass repetitively.
The simplest structure of a pillbox cavity is a cylinder with a radius a and a length l made of an good conducting material. In the case that the accelerating field E_z, where z is the direction of motion of the particle, and B_Θ

are the only electric and magnetic field components, the Maxwell's equations can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}(rB_\Theta) = \frac{1}{c^2}\frac{\partial E_z}{\partial t} \tag{1.4}$$

$$\frac{\partial E_z}{\partial r^2} = \frac{\partial B_\Theta}{\partial t} \quad . \tag{1.5}$$

Elimination of B_Θ yields

$$\frac{\partial^2 E_z}{\partial r^2} + \frac{1}{r}\frac{\partial E_z}{\partial r} = \frac{1}{c^2}\frac{\partial^2 E_z}{\partial t^2} \quad . \tag{1.6}$$

A solution for a mode with the angular frequency ω is

$$E'' + \frac{E'}{r} + \left(\frac{\omega}{c}\right)^2 E = 0 \quad . \tag{1.7}$$

This is a Bessel equation of zero order with the solution

$$E(r) = E_0 J_0\left(\frac{\omega}{c}r\right) \quad . \tag{1.8}$$

It was said that the cavity is made of a good conducting material, so the field has to vanish for $r = a$. This means that the argument of the Bessel function must be a zero point of J_0. The lowest frequency mode is associated with the first zero point

$$\frac{2\pi f}{c}a = 2.405 \quad . \tag{1.9}$$

An interesting value is the energy a particle gains when passing the cavity. Therefore a longitudinal electric field that is independent on the longitudinal coordinate z inside the cavity is considered, which yields

$$E_z(t) = \hat{E}_z \cos(\omega_{RF} t) \quad . \tag{1.10}$$

The coordinate for a particle passing through the cavity at an velocity v is $z = vt$. Along the length of the cavity l it gains a total energy of

$$\Delta W = \int_0^l q\hat{E}_z\left(\frac{\omega_{RF} z}{v}\right) dz = qV_0\frac{\sin\Theta}{\Theta} \tag{1.11}$$

with

$$\Theta = \frac{\omega_{RF} l}{v} \quad , \tag{1.12}$$

if $\hat{E}_z$ is replaced with the voltage amplitude V_0 inside the cavity and divided by the length l. This yields for the gained energy

$$\Delta W = qV_0T \tag{1.13}$$

and

$$T = \frac{\sin\Theta}{\Theta} \tag{1.14}$$

for the transit time factor.

By enhancing the cavity design by e.g. adding a nose cone to concentrate the electric field around the axis, the performance of the cavity can be improved. The eigenfrequency of such a cavity is a fix value. In order to tune the cavity e.g. a movable piston inside the cavity is used.

- **Ferrit–Loaded Cavities**

The concept of a pillbox cavity is in case of very long wavelength as well as fast tuning not appropriate. In order to build a cavity for long wavelength and that makes a fast tuning possible, the space inside of the cavity is filled for example with Ferrit ring cores. This is realized for the SIS–18 cavities at GSI. A more detailed description is given in section 2.1.

1.3.2 Electric Arcs in Cavities

Electric Arcs

Electric arcs are electrical discharges caused by a too high field gradient. Due to this a current flows through gas. Thereby the gas is ionized and a plasma channel is created.
An important mechanism describing this circumstance is Paschen's law:

$$V_B(pd) = \frac{Apd}{\ln(\frac{pd}{\text{atm}\cdot\text{m}}) + B} \tag{1.15}$$

It gives a relation between the product of gap distance d and gas pressure p on one side and the breakdown voltage V_B on the other side. The parameters A and B are constants depending on the properties of the gas used. For air, which is the gas that surrounds the gap of the cavity, $A = 43.6 \cdot 10^6 \frac{\text{V}}{\text{atm}\cdot\text{m}}$ and $B = 12.8$.

Triggers for Electric Arcs in Cavities

Triggers for electric arcs in cavities can have several different reasons:

- Dust and dirt in the cavity are changing the conductivity of the affected surfaces. Due to spikes in the electric flux lines and variations in the space charge distribution, an electric arc can be abetted.
- Humidity has got a strong influence on the dielectric strength of the air due to the influence on the conductivity.
- Change of the weather causing a low air pressure inside the housing of the cavity and leading to a lower breakdown voltage (cf. chapter 1.3.2).
- Cosmic radiation can lead to an ionization of the air inside the cavity.
- Natural radiation can also lead to ionization.
- Radiation caused by the operation of the accelerator acts like cosmic and radioactive radiation.
- Driving the cavity with a voltage exceeding the design value is an obvious, but also very important trigger for electric discharges.

Possible Damages

Possible damages to the cavity can be deformations of surfaces inside the cavity due to melting of material in case of persisting electric arcs. This can lead to a change of properties of the cavity and can cause malfunction.
A discharge inside the cavity leads to a damage of the gap periphery and can lead to failure. A case of burned cables at the gap of the SIS 18 cavity is documented in figure 1.5.

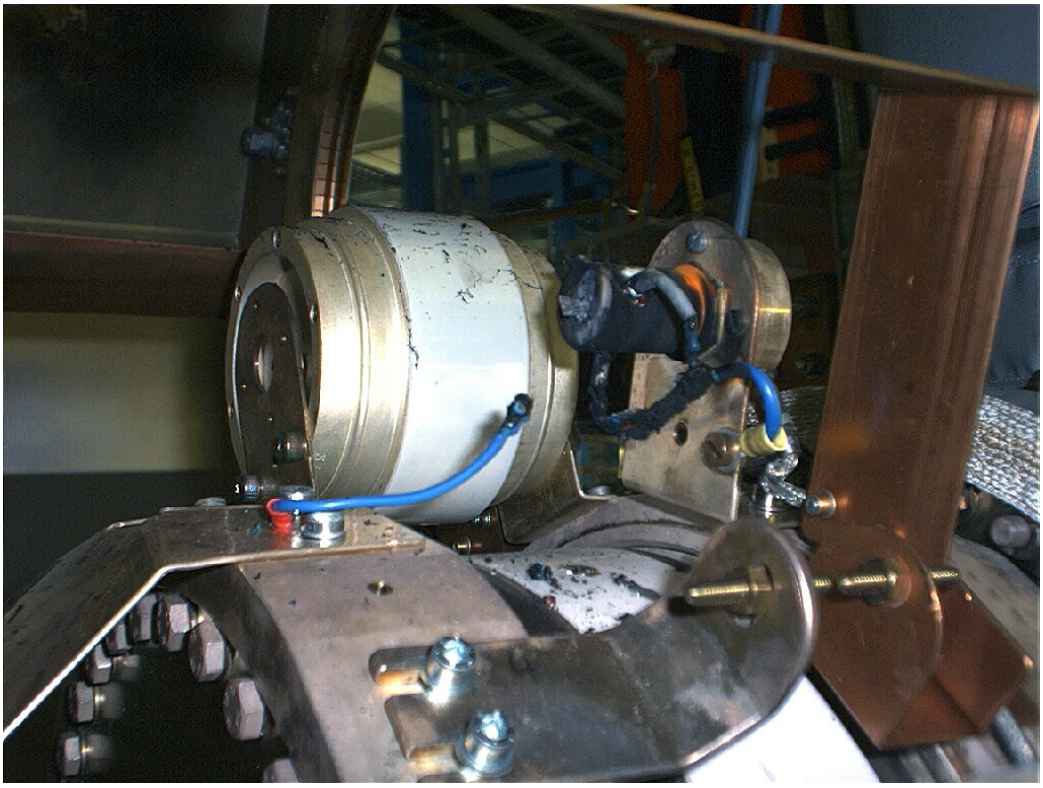

Figure 1.5: *Picture of the gap of the SIS 18 cavity after an ongoing electric arc. The arc moved due to thermodynamic effects from the predetermined point of flashover along the gap to a higher position and burned several cables.*

The burning was caused by an ongoing electric arc. Such an arc can, due to thermodynamical effects, move to a place located higher in comparison to the location of its origin. In this case the origin of the electric arc has been the predetermined point of flashover and it moved to the cables, which are located at a higher position.
In the case of an electric arc the functionality of the cavity is nullified, which leads in a synchrotron like the SIS 18 to beam loss and prevents further operation. This is because the amplitude of the gap voltage of the cavities and the magnetic field of the bending magnets are ramped simultaneously. While an electric arc is burning in the cavity, no acceleration is possible. An arc detector triggering a shutdown of the RF power cannot completely avoid, but drastically reduce such damages.

1.4 Machine Protection

In order to assure the safe operation of cavities several parameters have to be monitored and controlled. This include e.g. the temperature of cooling air and water as well as the checking if ventilators and pumps are functioning. All conditions leading to a possible damage of the system like e.g. ongoing electric arcs in a cavity have to be intercepted.

1.5 Arc Detection

In this chapter several methods for arc detection in acceleration cavities as well as for devices not related to particle accelerators are introduced.

1.5.1 Arc Detection Methods

- **Method for Arc Detection in Dynamoelectric Machines**

In [4] a method of detecting arcing faults in dynamoelectric machines is described. It is realized by monitoring the voltage on the neutral grounding. In case of an electric arc the produced RF voltages are detected by an RF voltage coupler and an RF monitor, which has a high impedance input amplifier.

- **Arc Detection Using Current Variation**

In [5] an arc detection method using current variation is described. It is realized by applying an AC line current to a load from an AC source of a given frequency producing repetitive cycles. An electric arc is detected by sensing cycle to cycle changes of the AC current.

- **Timing Window Arc Detection**

A method for arc detection for an electric circuit having an electrified conductor connecting a voltage source to a load is described in [6]. It is realized by detecting the electromagnetic field established by an electric arc with a field sensor. If a given timing characteristic is fulfilled, a trigger signal is produced.

1.5.2 Arc Detection in Cavities

The following three methods for electric arc detection have been proven at GSI. Detailed information is provided elsewhere [7].

- **Optical Monitoring**

By optical monitoring the electric arc is identified by measuring its emitted electromagnetic spectrum. For a test a photomultiplier (XP2972 by Photonis) has been used in a SIS–18 prototype cavity at GSI.

A similar method is realized in the low–level RF system of the compact energy recovery linac (cERL) at KEK (kou enerugii kasokuki kenkyuukikou, High Energy Accelerator Research Organization) by using an optical fiber and a photomultiplier–tube. The gain of each photomultiplier–tube is adjusted by using an light emitting diode attached to an adapter at the head of the fiber cable [8].

- **Measurement of the Impedance of the Cavity**

For the measurement of the impedance of the cavity a current transformer measures the RF current which with the cavity is driven. In addition the signal of the gap voltage is transfered to an analog device (IC AD 8302 [9]), which gives an output signal proportional to the impedance of the cavity. In comparison with an preset threshold an arc can be when the internal resistance of the cavity drops.

- **Comparison of Set and Actual Value**

The concept of the set–actual comparison, which is a variation of the measurement of the impedance of the cavity, is to compare the ratio of the gap voltage and the grid–1 voltage of the tetrode with a preset threshold. For the normal operation of the cavity without an electric arc

$$\frac{U_{gap}}{U_{g1}} > k_{lim} \cdot \frac{U_{gap,n}}{U_{g1,n}} \quad , \tag{1.16}$$

must hold, at which U_{gap} is the scaled gap voltage of the cavity (cf. chapter 2.1), U_{g1} is the scaled grid–1 voltage of the tetrode, $U_{gap,n}$ is the nominal gap voltage, $U_{g1,n}$ is the nominal grid–1 voltage and k_{lim} is a preset threshold. This method has been implemented in a LeCroy Wave Runner 44Xi oscilloscope for a test run. The input signals were tapped from the gap of a SIS–18

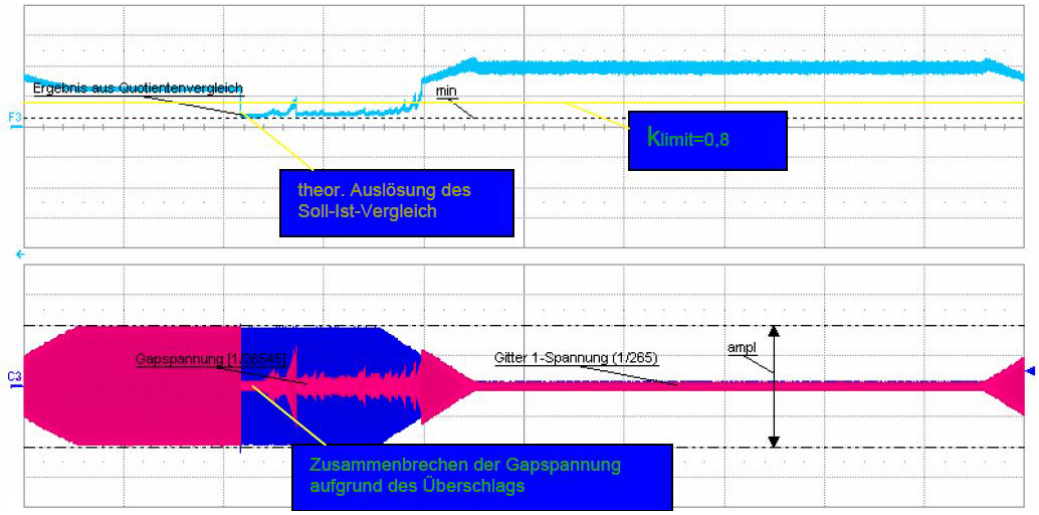

Figure 1.6: *Screen shot of a measurement during an electric arc occurring inside a SIS 18 cavity using a LeCroy Wave Runner 44Xi oscilloscope. In the lower plot the dark blue graph represents the grid–1 voltage of the tetrode, and the pink graph represents the gap voltage. For this measurement the feedback control of the cavity was turned off, and the grid–1 voltage amplitude has been limited. In the upper plot the light blue graph represents the gap–voltage–to–grid–1 voltage ratio, and the yellow line represents the preset threshold. In both plots voltage over time is plotted [7].*

cavity and from the grid–1 of the tetrode. Figure 1.6 shows a screen shot of a measurement during an electric arc occurring inside the cavity.

At a certain moment in time the gap voltage represented by the pink graph collapses and the ratio of gap and grid–1 voltage represented by the light blue graph drops below the threshold, which is marked by the yellow line. After this point in time the gap voltage fluctuates at a low level. Also the ratio fluctuates below the threshold. At the same time the voltage of grid–1 remains at maximum amplitude, which means inside the cavity there is an ongoing electric arc burning.

After a certain amount of time the grid–1 voltage is ramped down. At about the middle of the maximum amplitude the gap voltages stops fluctuating and follows the grid–1 voltage. Simultaneously the computed ratio rises above the threshold, which means the electric arc inside the cavity stopped burning.

1.6 Structure of the Thesis

In this thesis the new development, realization, and test testing of an FPGA–based are detector for cavities is presented. Therefore in chapter 2 an overview of the SIS–18 radio frequency system at GSI is given. The requirements for the arc detector following from this are shown in chapter 3. In order to realize the chosen detection method, the amplitudes of the RF signal of the control grid of the tetrode and of the gap of the cavity have to be determined. The theoretical background for this is introduced in chapter 4. In chapter 5 the design, development, and actual realization of the arc detector is described. Chapter 6 deals with the verification of the functionality of the arc detector within a test environment including the measurements of its characteristics and an overview of the rest readings. The application of the arc detector in a SIS–18 prototype cavity as well as the error analysis of the result of the test run is presented in chapter 7. In chapter 8 a summary of the thesis and future prospects are given.

Chapter 2

Overview of the SIS–18 Radio Frequency System

2.1 Functionality of the SIS 18 Cavity

The SIS 18 RF cavity is a coaxial double resonator in which two stationary $\frac{\lambda}{4}$ waves are generated [10]. Figure 2.1 shows a diagram of the cavity.

Inside the cavity there is the stainless steel vacuum beam pipe electrically separated by a ceramic gap representing a constant capacitance. Around the beam pipe on the left and on the right–hand side of the ceramic gap ferrite ring cores made of FX8C12 ferrite featuring a high magnetic permeability are installed. The inductance of the ring cores depends on the permeability, which can be altered by a superimposed magnetic field driven by a current from 0 to 800 A [11] that flows through the bias windings around the ring cores to tune the resonance frequency of the cavity.
The expression of the resonance frequency f_r is

$$f_r = \frac{1}{2\pi\sqrt{L(\mu_r) \cdot C_{Total}}} \quad . \tag{2.1}$$

Thereby L is the inductance of the ring cores depending on the magnetic permeability μ_r and C_{Total} the capacitance of the cavity.
The frequency of the SIS 18 RF system ranges from 0.8 to 5.4 MHz and for the SIS–100 acceleration system from 1.1 to 2.8 MHz.
For monitoring purposes the gap voltage is tapped and scaled down by a voltage divider.
The cavity is powered by a tetrode power amplifier whose driver signal is generated by a DDS (Direct Digital Synthesis) module and an amplitude

modulator. The electric power is coupled into the cavity by an inductive as well as capacitive path.
For measuring the amplitude and phase of the wave inside the cavity for the amplitude–feedback loop and for the phase–feedback loop, the usage of a combination of a FIB (FPGA Interface Board) and a FAB (FIB Adapter Board) is planned [12].
Also for electric arc detection the measurement of voltage amplitudes is required. Hence a similar hardware configuration can be used for realizing an arc detector.

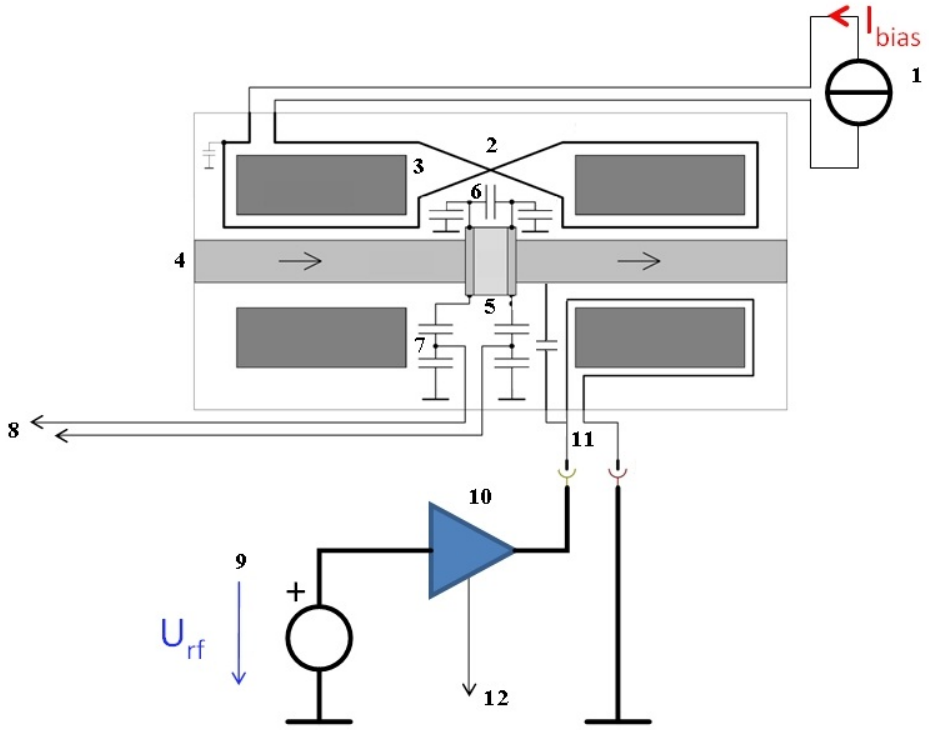

Figure 2.1: *Diagram of SIS 18 cavity including current source for bias windings (1), bias windings (2), ferrite ring cores (3), beam pipe (4), ceramic gap (5), capacitors for adjusting frequency range of the cavity (6), voltage divider (7) for gap voltage monitoring (8), voltage source (9), tetrode amplifier to power the cavity (10), mixed coupling (11) and output for monitoring grid–1 voltage of the tetrode (12). [11]*

2.2 FPGA Interface Board

The FIB is a multipurpose board consisting mainly of an FPGA and several interfaces. It has been developed by the RF group at GSI. Figure 2.2 shows a picture of the FIB. Table 2.1 lists the interfaces.

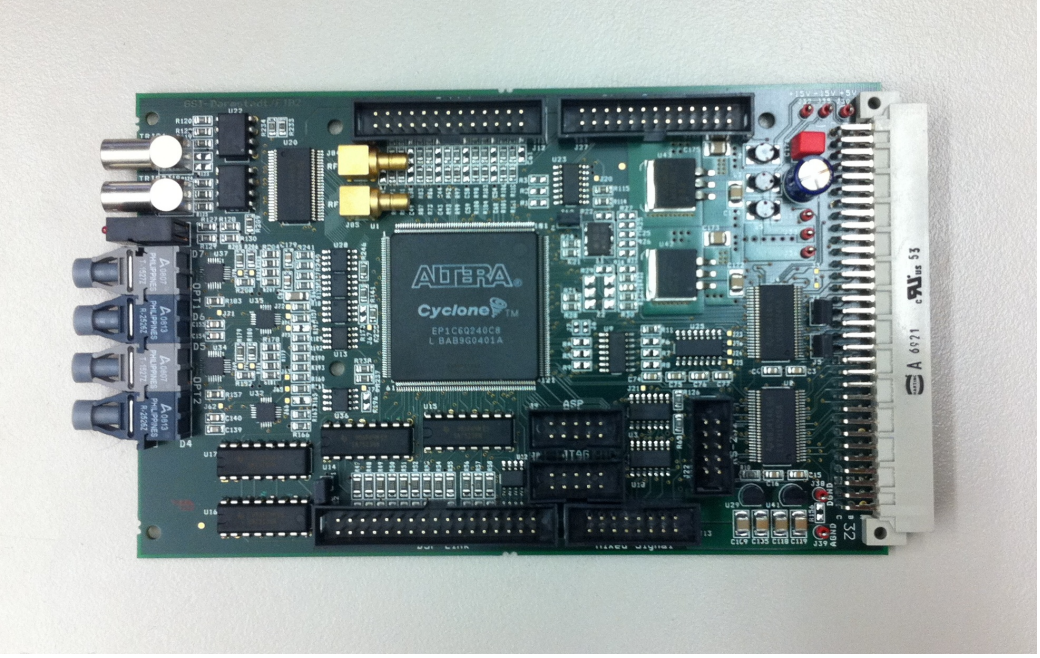

Figure 2.2: *Picture of the FIB (FPGA Interface Board). On the left hand side two LEMO plugs, four LED for displaying a status code, and four optical I/Os. In the center a Cyclone FPGA by Altera. On top and bottom there are several interfaces, see 2.1 for a list. On the right hand side the interface for connecting the FIB to the backplane.*

The FPGA used is a Cyclone (EP1C6Q240-C8) from Altera. It belongs to the EP1C6 series, which means it comes with 92160 RAM Bits (11520 Byte), 5980 logic cells and 240 pins (185 input–output pins and 55 for voltage supply, clocking and configuration). It also provides 2 PLL (Phase–Locked Loop) units for producing other frequencies. The switching speed is 8 ns with a maximum clocking frequency of 275 MHz. The clocking frequency of the FPGA for the usage on the FIB is set to 50 MHz [12, 13].

Interface	Purpose
DSP link	Parallel, unidirectional 8 bit high–speed interface, max. 40 Mbit/s
μC link	Parallel 8 bit interface for a micro–controller or a FAB
Piggy connector	Parallel 8 bit interface for FAB
Control system backplane	Parallel 24 bit interface to central accelerator control system
2 RF clock input	For external clocking, max. 100 MHz
2 optical Versa link interfaces (2 emitters and 2 receivers each)	Serial optical interface, max. 40 Mbit/s
RS–232, ASP and JTAG interfaces	Serial interfaces for configuration and diagnosis via PC

Table 2.1: *Table of interfaces on the FIB [12]*

Figure 2.3 shows a schematic of the FIB including only the elements important for the application in the scope of this work.

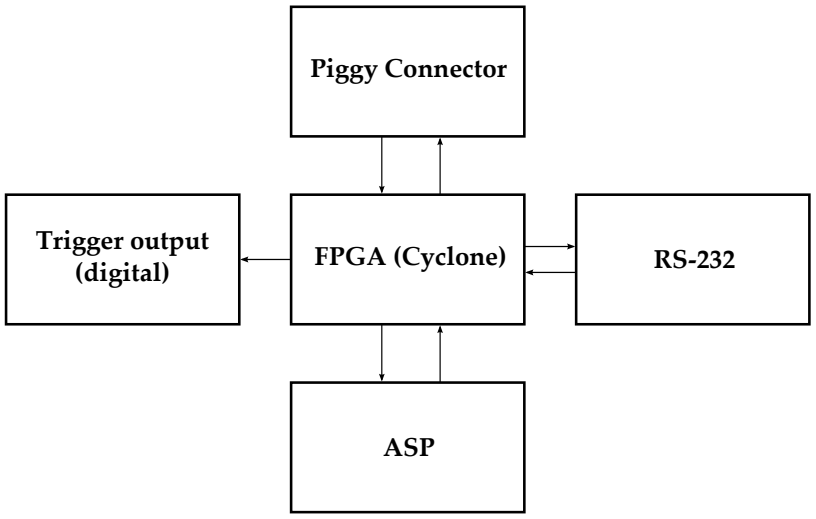

Figure 2.3: *Schematic of the FIB: The FIB provides a piggy–connector as an interface for communication with a FAB. All incoming data is processed by the FPGA. A digital trigger signal generated by the FPGA can be sent over a LEMO interface. Programming the FPGA can be done via the ASP interface. The RS–232 interface is used for communication with a PC.*

2.3 FIB Adapter Board

FABs are extension boards for the FIB. For the arc detector an ADC/DAC FAB is used. It is also a design developed by the RF group at GSI. Figure 2.4 shows a picture of it.

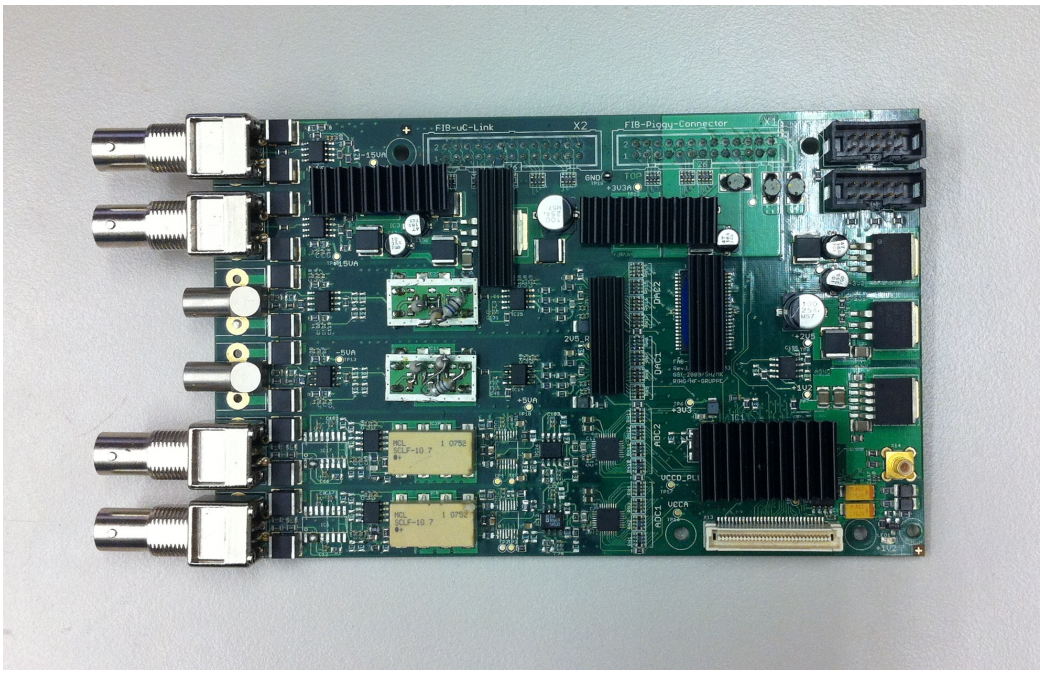

Figure 2.4: *Picture of the ADC/DAC FAB (FIB Adapter Board). On the left hand side from top to bottom two BNC plugs for monitoring the ADC input signals, two LEMO plugs for output, and two BNC plugs for AC input. Top right two programming interfaces for ASP and JTAG. Bottom right a FPGA Cyclone III covered by a cooler.*

The FIB is connected to the FAB via a μC–Link and a piggy–connector. The ADC/DAC FAB provides two analog/digital input interfaces (BNC connectors), two digital/analog output interfaces (LEMO connectors) and two ADC monitoring interfaces (BNC connectors). These analog I/Os can be assembled for AC or DC operation, depending on the purpose. The input interfaces are configured for AC operation for their use in the arc detector setup.
The ADC used on the ADC/DAC FAB provides a resolution of 14 bit and a sampling frequency of 105 MHz. The DAC has a resolution of 14 bit and a maximum data transfer rate of 210 MSPS [12].

Beside this it comes with an FPGA and for this reason also with an ASP (Active Serial Programming) and JTAG (Joint Test Action Group) interface for programming and diagnostics via PC (Personal Computer). The FPGA is a Cyclone III (EP3C25F256I7N) from Altera. Its main features are 4 PLL units and 564 kbit of RAM.
See figure 2.5 for a schematic of the FAB showing only the elements important for the application in the scope of this work.

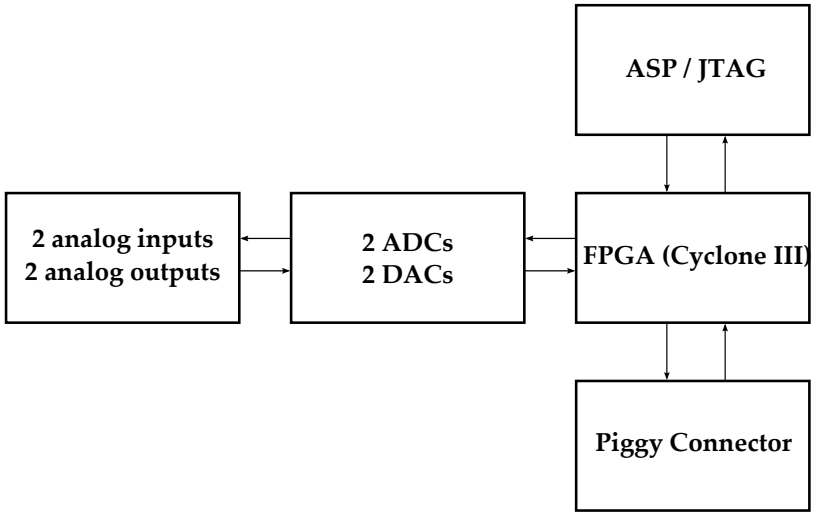

Figure 2.5: *Schematic of the FAB: The FAB provides two BNC plugs for analog input signals, which are digitized by two ADCs. The digital signals are sent to the FPGA where they are processed. Digital signals generated in the FPGA can be transformed into analog signals and can be taped over two LEMO plugs. The the piggy connector is for communication with the FIB. Programming and diagnostics of the FPGA can be done via the ASP and JTAG interfaces.*

2.4 Existing Arc Detector

The steepness of the trailing edge of the gap voltage amplitude was evaluated in order to detect electric arcs.
Due to the quality factor of the cavity ($Q \approx 8$ at $f = 800$ kHz and $Q \approx 60$ at $f = 6$ MHz) the amplitude of the gap voltage does not drop to zero instantly. Dropping times are in the order of $\tau_{drop} \approx 10$ μs. If the dropping time is below this, it is usually an indicator for an electric arc. This is because the

energy usually stored in the cavity is dissipated in the electric arc.
To detect this, the arc detector receives a signal of the actual value of the amplitude from the amplitude detector. If the signal drops faster than 2.5 kV/μs, an electric arc is claimed to be detected. The principle is illustrated in figure 2.6.
The output signal of the arc detector that is delivered to the interlock lies usually at a level of 15 V. In the case of an electric arc it drops to 0 V.

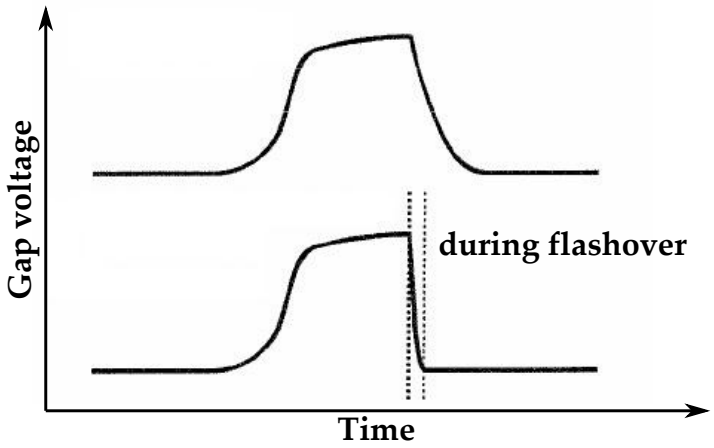

Figure 2.6: *Characteristics of the amplitude without (upper graph) and during an electric arc (lower graph). The dotted lines indicate the time interval in which the voltage drops during a flashover. [7]*

The RF–voltage is turned off in two steps:

- The amplitude controller receives an interlock signal and stops providing an output signal.
- The drive amplifier is turned off and the short–circuiting device for the gap is activated.

The shutdown of the driver is displayed in the main control room and the cavity is marked as inactive.

2.5 Motivation for the New Development

So far electric arcs in the cavities have been detected by measuring the falling edge of the amplitude of the gap voltage. This method is error–prone in case of steep ramps and for lowering of the eigenfrequency of the cavity below 800 kHz, what is a demand for the new storage rings.
Hence a new method that is as easy and reliable as possible had to be found. Such a detector will be used for the ferrite– and MA–cavities (Metallic Alloy) in the SIS 18, SIS 100 and storage rings in FAIR [7].

Chapter 3

Requirements of the New Arc Detector

This work aims at constructing, implementing, and testing a reliable detector for electric arcs for the accelerating cavities that are used at GSI. The arc detector used so far does not detect arcs reliably (cf. chapter 2.5). Several potential methods for arc detection have been rated. Thereby it turned out realizing the method of set–actual comparison with a digital FPGA–based (Field Programmable Gate Array) arc detector including a new development fit the demands best. Therefore already existing hardware at GSI can be used. Also all required signals (gap voltage and grid–1 voltage) are already available in the RF–system cabinets, so no additional sensors or hardware have to be implemented [7]. In order to be compatible with the SIS 18 cavity control system the arc detector has to fulfill the specifications given in table 3.1.

Two analog input channels are needed for tapping the gap voltage of the accelerator cavity and the control grid (grid–1) voltage of the corresponding tetrode. Those voltages are divided down to a level of 10 dBm. The frequency ranges of all the cavities installed in the different accelerator facilities are in a range of (0.4 - 6) MHz. In case of an electric arc a trigger signal has to be generated. The overall response time of the detector should be less then 1 ms to prevent an ongoing electric arc. Because the arc detector will be used within different systems the threshold (cf. chapter 1.5.2) has to be adjustable. This adjustment has be done by configuring the FPGA using the RS–232 interface. In addition it is desirable to include the functionality of an amplitude detector.
These requirements allow an operation of the arc detector in the currently used analog control system of the cavity as well as in the planned digital control system of the future FAIR facility. Figure 3.1 shows a simple block

Category	Required values
Input	2 analog channels
Input voltage	$\leq$ 10 dBm
Input frequency range	(0.4 – 6) MHz
Dynamic range of ADC1 channel	16.5 dB
Dynamic range of ADC2 channel	16.5 dB
Variation of frequency response of ADC1 channel	6 %
Variation of frequency response of ADC2 channel	6 %
Output	1 digital trigger channel (0 - 5) V
Response time	$<$ 1 ms
Configurability	via RS–232

Table 3.1: *Required specifications of the arc detector*

diagram of the feedback control system.

The project will be finished with the confirmation of application of the arc detector within a test setup and the confirmation of application in a SIS 18 prototype cavity.

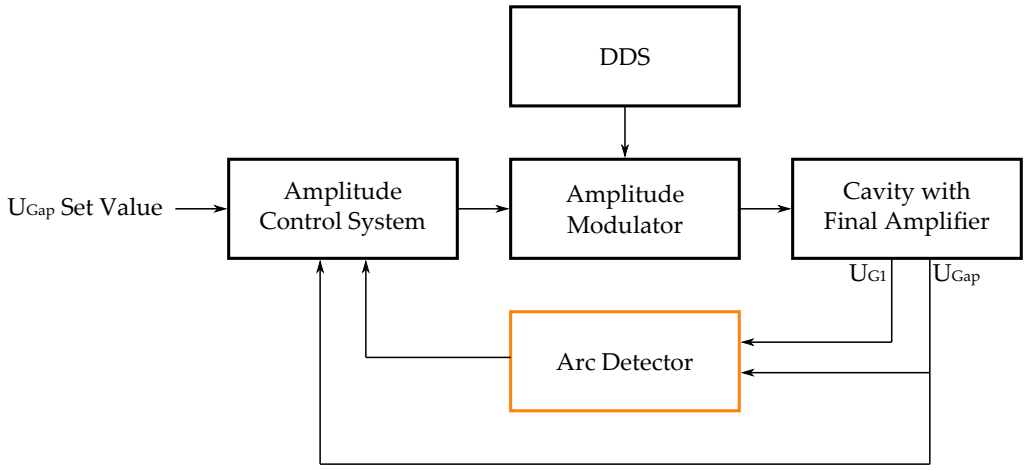

Figure 3.1: *Block diagram of feedback control system: A set value for the gap voltage is sent to the amplitude control system. According to the actual value of the gap voltage it generates a set value that is sent to the amplitude modulator, which generates together with a DDS (Direct Digital Synthesis) an RF signal. This is sent to the final amplifier that is driving the cavity. The gap voltage amplitude and the grid–1 voltage amplitude are tapped and sent to the arc detector. In case of an electric arc it sends an interlock signal to the amplitude control system.*

Chapter 4

Theoretical Background of Amplitude Detection

In order to implement the method introduced in chapter 1.5.2 in an FPGA, the amplitudes of the gap voltage of the cavity and of the grid–1 voltage of the respective tetrode have to be determined. This can be accomplished by using the CORDIC (COordiante Rotation DIgital Computer) algorithm in combination with a time discrete Hilbert transform [12].
The Hilbert transform is used to shift the input signal, which is a stepwise sine provided by the respective ADC, by 90°. This has to be done because the CORDIC algorithm can only process a signal consisting of both a real and an imaginary part. The original signal represents the real part and the signal shifted by 90° represents the imaginary part.
As a following step the CORDIC algorithm is applied to both signals, which yields the phase and the amplitude of the input signal.

4.1 Hilbert Transform

4.1.1 Hilbert Transform Continuous in Time

The Hilbert transform $H\{f\}$ of a function f is defined as

$$g(t) = H\{f(t)\} = \frac{1}{\pi} \int_{-\infty}^{\infty} \frac{f(\tau)}{t-\tau} d\tau \quad . \tag{4.1}$$

The inverse Hilbert transform that allows the calculation of the original function $f(t)$ is given by

$$H^{-1}\{g(t)\} = -H\{g(t)\} = f(t) \quad . \tag{4.2}$$

The Hilbert transform can also be written as a convolution with the function $\frac{1}{\pi t}$

$$g(t) = H\{f(t)\} = \frac{1}{\pi t} * f(t) \quad . \tag{4.3}$$

The Fourier transform of $\frac{1}{\pi t}$ yields the transfer function

$$F\left\{\frac{1}{\pi t}\right\} = -i \cdot \mathrm{sgn}(\omega) = e^{-i\frac{\pi}{2}\mathrm{sgn}(\omega)} \quad . \tag{4.4}$$

The frequency response of this transfer function is plotted in figure 4.1.

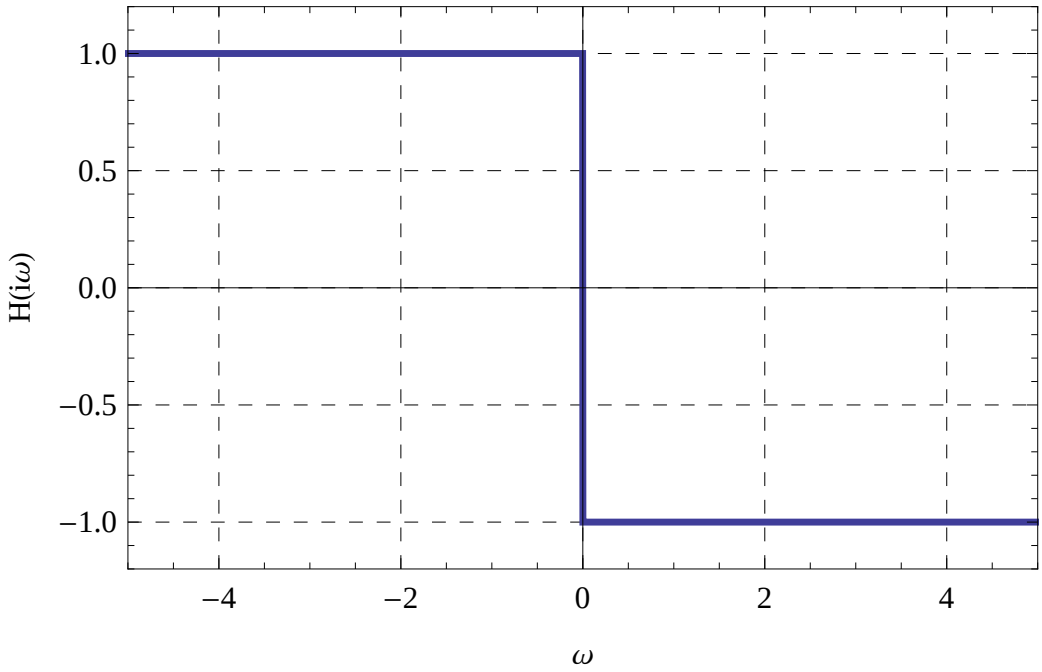

Figure 4.1: *Plot of the frequency response of the Hilbert transfer function.*

The convolution from equation (4.3) can be expressed by a product in the frequency domain

$$\hat{g}(i\omega) = \hat{f}(i\omega) \cdot -i \cdot \mathrm{sgn}(\omega) \quad . \tag{4.5}$$

Example functions and the respective Hilbert transform are listed in table 4.1. For detailed information see [14, 15].

	$f(t)$	$H\{f(t)\}$
Constant	a	0
Dirac delta	$\delta(t)$	$\frac{1}{\pi t}$
Sine	$\sin(\omega t)$	$-\cos(\omega t)$
Cosine	$\cos(\omega t)$	$\sin(\omega t)$

Table 4.1: *Table of several functions and their Hilbert transform.*

4.1.2 Hilbert Transform Discrete in Time

Due to the clocking of the FPGA, the Hilbert transform in VHDL cannot be done continuously, but discrete steps in time have to be taken. Another constraint is that due to a limited calculating capacity only a certain bandwidth can be processed with an FPGA. The bandwidth will fulfill the requirements shown in table 3.1.
Is the sampling rate at least twice the limitation in bandwidth, the Nyquist–Shannon sampling theorem [16] is fulfilled. Hence a sequence $g[k]$ discrete in time can be generated without loss of information about the original signal. Thereby k is a positive integer, and a Hilbert transform discrete in time can be written as

$$H\left\{g[h]\right\} = h[k] * g[k] \quad . \tag{4.6}$$

The impulse response $h[k]$ is

$$h[k] = \frac{1-\cos(\pi k)}{\pi k} = \begin{cases} \frac{2}{\pi k} & \text{if } k \text{ odd} \\ 0 & \text{if } k \text{ even} \end{cases} \quad . \tag{4.7}$$

The Hilbert transform discrete in time is not causal [12].

4.2 CORDIC Algorithm

The signal generated using the time discrete Hilbert transform can be interpreted as a vector in the complex plane. To derive the absolute value of it, the arc tangent or squaring and computing the square root can be used. These methods are very compute bound and time–consuming on FPGAs. The CORDIC (COordiante Rotation DIgital Computer) is a fast alternative to these methods.
It is derived from the general rotation transform of a 2–component vector

$$\begin{pmatrix} x' \\ y' \end{pmatrix} = \begin{pmatrix} \cos(\phi) & -\sin(\phi) \\ \sin(\phi) & \cos(\phi) \end{pmatrix} \begin{pmatrix} x \\ y \end{pmatrix} \tag{4.8}$$

which rotates the vector by the angle ϕ in the Cartesian plane. For an iterative rotation, equation (4.8) can be rewritten as

$$\begin{pmatrix} x_{i+1} \\ y_{i+1} \end{pmatrix} = \begin{pmatrix} \cos(\phi_i) & -\sin(\phi_i) \\ \sin(\phi_i) & \cos(\phi_i) \end{pmatrix} \begin{pmatrix} x_i \\ y_i \end{pmatrix} \quad . \tag{4.9}$$

A simple rearrangement in which $\cos(\phi_i)$ is treated as a scalar yields

$$\begin{pmatrix} x_{i+1} \\ y_{i+1} \end{pmatrix} = \cos(\phi_i) \begin{pmatrix} 1 & -\tan(\phi_i) \\ \tan(\phi_i) & 1 \end{pmatrix} \begin{pmatrix} x_i \\ y_i \end{pmatrix} \quad . \tag{4.10}$$

Now the amount of multiplications is reduced from four to three. If the rotation angles are restricted so that

$$\tan(\phi_i) = \pm 2^{-i} \tag{4.11}$$

the multiplication with the tangent term can be translated into shift operation. Thus a rotation by an arbitrary angle ϕ can be expressed by a sum of rotations by the angles ϕ_i

$$\phi = \sum_{i=0}^{\infty} S_i \phi_i \quad , \tag{4.12}$$

where S_i is the sign of the angle. Using this, equation (4.11) yields

$$\tan(\phi_i) = S_i 2^{-i} \tag{4.13}$$

and equation (4.10) can be rewritten as

$$\begin{pmatrix} x_{i+1} \\ y_{i+1} \end{pmatrix} = \cos(\phi_i) \begin{pmatrix} 1 & -S_i 2^{-i} \\ S_i 2^{-i} & 1 \end{pmatrix} \begin{pmatrix} x_i \\ y_i \end{pmatrix} \quad , \tag{4.14}$$

where $\cos(\phi_i)$ can be treated as a constant because there is no change in sign due to the fact that $\cos(\phi_i) = \cos(-\phi_i)$. This constant can be calculated by

$$K = \prod_{i=0}^{\infty} \cos(\arctan(2^{-i})) \approx 0.607 \quad . \tag{4.15}$$

This holds for an infinite amount of iterations. Due to that constant the algorithm has a gain of approximately 1.647.
Now the angles between ϕ and the steps of the iteration can be written as

$$\phi_{i+1} = \phi_i - S_i \cdot \arctan(2^{-i}) \quad . \tag{4.16}$$

Figure 4.2 shows a sketch of the principle. In order to compute the amplitude the CORDIC algorithm has to be operated in rotation mode [17]. In this mode the CORDIC algorithm rotates the input vector so that it is aligned to the x axis. This also means minimizing the y component of the residual vector at each step of the rotation. The residual y component y_i is used to determine the direction of rotation.

$$S_i = \begin{cases} +1 & \text{if } y_i < 0 \\ -1 & \text{else} \end{cases} \quad . \tag{4.17}$$

This leads to

$$x_n = A_n \sqrt{x_0^2 + y_0^2} \tag{4.18}$$

and

$$y_n = 0 \quad , \tag{4.19}$$

with $A_n = \prod_n \sqrt{1 + 2^{2i}}$. Thereby x_n represents the amplitudeee [12, 17].

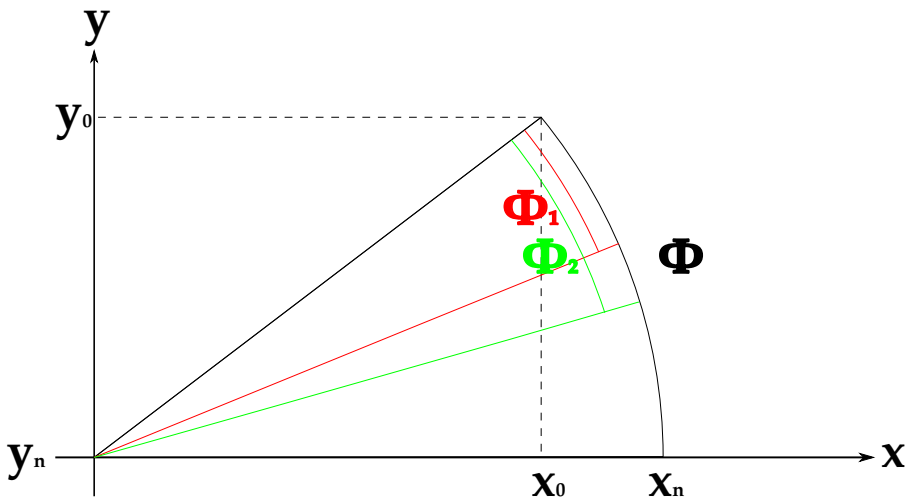

Figure 4.2: *CORDIC algorithm in rotation mode. The input vector (black) with the components x_0 and y_0 and an angle of ϕ is rotated to align the x axis. This is done in steps of an iteration yielding vectors with an angle of ϕ_1 (red), ϕ_2 (green), and so on. After a sufficient amount of steps the vector is aligned to the x axis at which x_n represents the amplitude of the original input vector.*

Chapter 5

Realization of the Arc Detector

5.1 Reconfiguration of Hardware

In order to provide an excellent input signal to the ADCs, the hardware configuration had to be changed.
In figures A.1 and A.2 in appendix A one can see the original configuration of the FAB. All changes that were made are listed in table 5.1.

Component	Original value	New value
R11	510 Ω	110 Ω
R13	1 kΩ	open
R14	0 Ω	open
R16	0 Ω	open
R52	0 Ω	100 nF
R64	1 kΩ	open
R65	0 Ω	open
R66	0 Ω	open
R71	0 Ω	100 nF
R72	open	0 Ω
R73	open	0 Ω
R92	510 Ω	110 Ω
C28	100 nF	open
C30	100 nF	open
C104	100 nF	open
C105	100 nF	open

Table 5.1: *Changes to the FAB hardware configuration*

Figure 5.1 shows a block diagram of the analog signal processing on the FAB before and after the the reconfiguration.

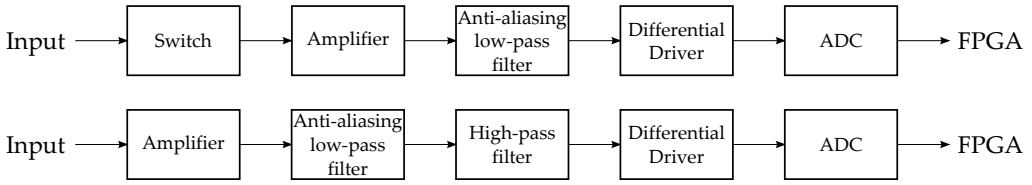

Figure 5.1: *Block diagram of analog signal processing on FAB before (top) and after (bottom) reconfiguration: The switch has been disabled. It allowed to choose a signal of constant 2.5 V or ground to be processed by the following components. After the reconfiguration the input signal is amplified by an amplifier and filtered by an anti–aliasing low–pass filter. This is done to ensure that the Nyquist–Shannon sampling theorem [16] at the ADC is fulfilled. A high-pass filter has been implemented for blocking the DC part of the signal. The differential driver provides the input signal for the ADC that digitizes the signal and sends it to the FPGA.*

In addition to the changes on the board a 6dB DC–4 GHz 50 Ω attenuator has been plugged in the input jack to scale down the input signal to the required amplitude.
It turned out that the VGAs (Variable Gain Amplifier) produced a not negligible noise. Because of this parts of the input circuit have been removed in order to exclude the VGAs in the circuit.
With the other changes an input voltage of 1.5 V_{PP} for the ADCs, which is their maximal input voltage, at an input level of 11 dBm at the BNC input plug was set. This yields 1 dBm of safety margin for the input level.

5.2 Implementation of the Algorithm for Arc Detection in VHDL

The framework for realizing and implementing a VHDL algorithm on the FIB (cf. chapter 2.2) and FAB (cf. chapter 2.3) hardware that meets all specifications consists of two programming parts: one for the FAB and one for the FIB. Both parts provide the respective packages needed for communication via I/O interfaces, FUB–conform (FPGA Universal Bus) FPGA internal communication (cf. chapter 5.2.4), signal conversion, and signal processing.

One package in the FAB detector framework is the arc detector core (cf. chapter 5.2.2) which is the main item of the whole algorithm. In this package the detection of an arc depending on several settings is implemented.

5.2.1 Design of the Detector Framework

The hardware of the FIB and the FAB comes with several I/O interfaces implemented. The buildup of packages that are required to operate the two ADC channels, the two DAC channels, the flash memory, the RAM, and the piggy interface as well as to process signals on the FAB is called FAB detector framework. Correspondingly, all packages needed for operation of the trigger output channel, the RS–232 interface, and the piggy interface on the FIB is called FIB detector framework. Both parts are called the detector framework. Figure 5.2 shows a schematic of the detector framework including all used packages. In the following a detailed explanation of the layout and functionality is given.

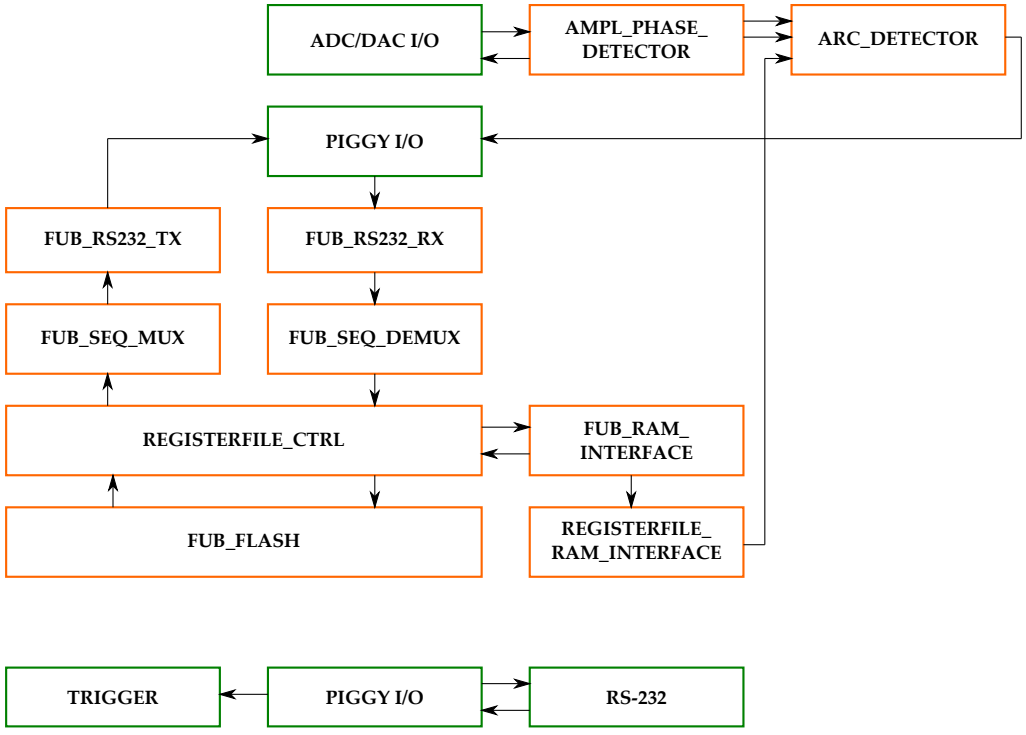

Figure 5.2: *Schematic of detector framework: The upper schematic shows the principle of the program segment for the FAB, the lower one for the FIB. Ports are illustrated in green, packages in orange.*

FAB Detector Framework

The analog voltage signals from the gap of the cavity and from grid–1 of the tetrode are digitized by two ADCs. Thereby the gap signal is assigned to channel 1 and the grid–1 signal to channel 2. Both digital signals have a sine wave–form while the cavity is driven, otherwise the signals are constants around zero. These signals are fed to the package of the amplitude and phase detector called AMPL_PHASE_DETECTOR. The signals are also sent to two DACs. There the assignment of channel 1 and channel 2 is consistent to the ADC channels.
At the input–ports of the amplitude and phase detector package the offset of the signals can be adjusted separately on demand. These arbitrary offsets are defined by values, which are read from a register file (see below). The signals are processed by a Hilbert transformator (cf. chapter 4.1.2) and the CORDIC algorithm (cf. chapter 4.2) in order to compute the amplitudes and the phase difference of both signals. In the case of the arc detector only the information about the amplitudes of the signals is sent to the arc detector core (cf. chapter 5.2.2).
The ARC_DETECTOR (arc detector core) is the package that sends out a trigger signal when an arc occurs in the cavity. The characteristics of the triggering depend on settings, which can be configured via the register file (see below). The trigger signal is sent to the piggy interface and therewith to the FPGA on the FIB, on which the FIB detector framework is runs.
The data sent via the RS–232 interface from a PC is directed within the FIB detector framework to the piggy connector and transferred to the FAB detector framework. It is received by the package called FUB_RS232_RX.
The package FUB_SEQ_DEMUX demultipexes the received data. This means it converts the serial RS–232 to a parallel data format, which is called FUB 5.2.4 and is used for the internal communication between the packages. Afterwards the data is passed to the package REGISTERFILE_CTRL (registerfile control).
The register file control manages the data streams for writing and reading data to the flash memory via the package FUB_FLASH, for writing and reading data to the RAM via the package FUB_RAM_INTERFACE, and for sending data via RS–232 back to a PC. In the last case the data is multiplexed by the package FUB_SEQ_MUX, sent by the package FUB_RS232_TX to the piggy I/O, and on this way directed over the FIB to the RS–232 plug.
The data that is written by the registerfile control into the RAM can be accessed by the package REGISTERFILE_RAM_INTERFACE. It provides a signal named register file that has the format of a binary sequence. The register file is sent to the packages of the amplitudes and phase detector as well

as to the arc detector core. By writing data via RS–232 to the register file the amplitude and phase detector and the arc detector core can be configured.

The whole detector framework was designed to be used as a multipurpose framework. By replacing the arc detector core with another core nearly every type of detector that needs one or two ADC input channels, a trigger output channel, and up to two DAC output channels can easily be realized. In the current configuration amplitudes of sign wave–forms and differences in phase can be detected. By leaving out the amplitude and phase detector package also detectors for levels can be realized.

FIB Detector Framework

The layout of the FIB detector framework consists of the unidirectional connection between the piggy I/O and the trigger output channel as well as the bidirectional connection between the piggy I/O and the RS–232 interface only. The FPGA on the FIB is not used for any signal processing. It only ensures signal transmission.

5.2.2 Design of the Arc Detector Core

The arc detector core is the main item of the implemented algorithm. It generates a trigger signal in case of an arc occurring in the cavity. Figure 5.3 shows a schematic of the arc detector core (cf. chapter 6).

The input signals for the arc detector core are two signed 15–bit logic vectors, which are carrying information about the amplitude of the gap voltage of the cavity (adc_1_amp_i) and the grid–1 voltage of the tetrode (adc_2_amp_i). Both signals are converted into fixed–point 30–bit logic vectors, in which the point is in the exact middle of the vectors. After the conversion the ratio of the gap voltage and the grid–1 voltage is computed by using a divider.
In a following step it is checked whether the grid–1 voltage exceeds a preset threshold called the grid–1 voltage limit (ug1lim). This threshold is set via the register file (register_io) with a default value of 15% of the maximal amplitude that can be detected. If the threshold is exceeded, the ratio will be written to a 30–bit logic vector signal (adc_1_adc_2_quotient_afterhold). Otherwise the ratio will be sampled and held. This is to mask out signals with low amplitudes and noise when there are no input signals.
After this the signal (adc_1_adc_2_quotient_afterhold) is mixed by using a multiplier with a 30–bit signal (impset) that can be set via the register file depending on the impedance of the cavity. The default value is 10000 in

decimal notation. This feature is added for future projects in preparation for real–time monitoring of the impedance of the cavity.
The fixed–point multiplication yields a 60–bit signal (impscaled), which is filtered by a finite impulse response (FIR) low–pass filter in order to reduce noise. The FIR–low–pass filter is realized by writing the signal continuously in an array that contains sixteen samples. During every clock the contents of the array is shifted in such a way that at the first position always is the latest sample. Also every clock the mean value of the signals in the array is computed what yields the low–pass filtered signal (quotient).
Via the register file a threshold (zlim_set) can bet set. The default value is 80% of the ratio of the nominal gap voltage and the grid–1 voltage, thus the default value is set to 0.8 in decimal notation. This threshold is multiplied with the set value (impset) so that the threshold and the ratio have the same scale. If the ratio signal falls below the threshold (zlim), the trigger signal (trigger) is set to logic one. If not, it is set to logic zero.
the trigger output signal (trigger_o) is set to logic zero, if both amplitude signals of the gap voltage (adc_1_amp_i) and grid–1 voltage (adc_2_amp_i) are falling below the the grid–1 voltage limit (ug1lim). This is to assure that there is no trigger signal sent after the drop down of the voltage signals disregarding their sequence.
The trigger output signal (trigger_o) is sent from the arc detector core package directly via the piggy I/O to the trigger output on the FIB. If the voltage signals exceed the grid–1 voltage limit and a trigger signal is generated, the trigger signal will be sampled and held for a preset time by using a monostable flipflop. The preset time can be set via the register file. The default value is 1 second. This is to avoid a continuous and fast switching of the trigger output signal (trigger_o), which can occur when the ratio is close to the threshold, in order to prevent damage of the control system hardware that is connected to the arc detector.

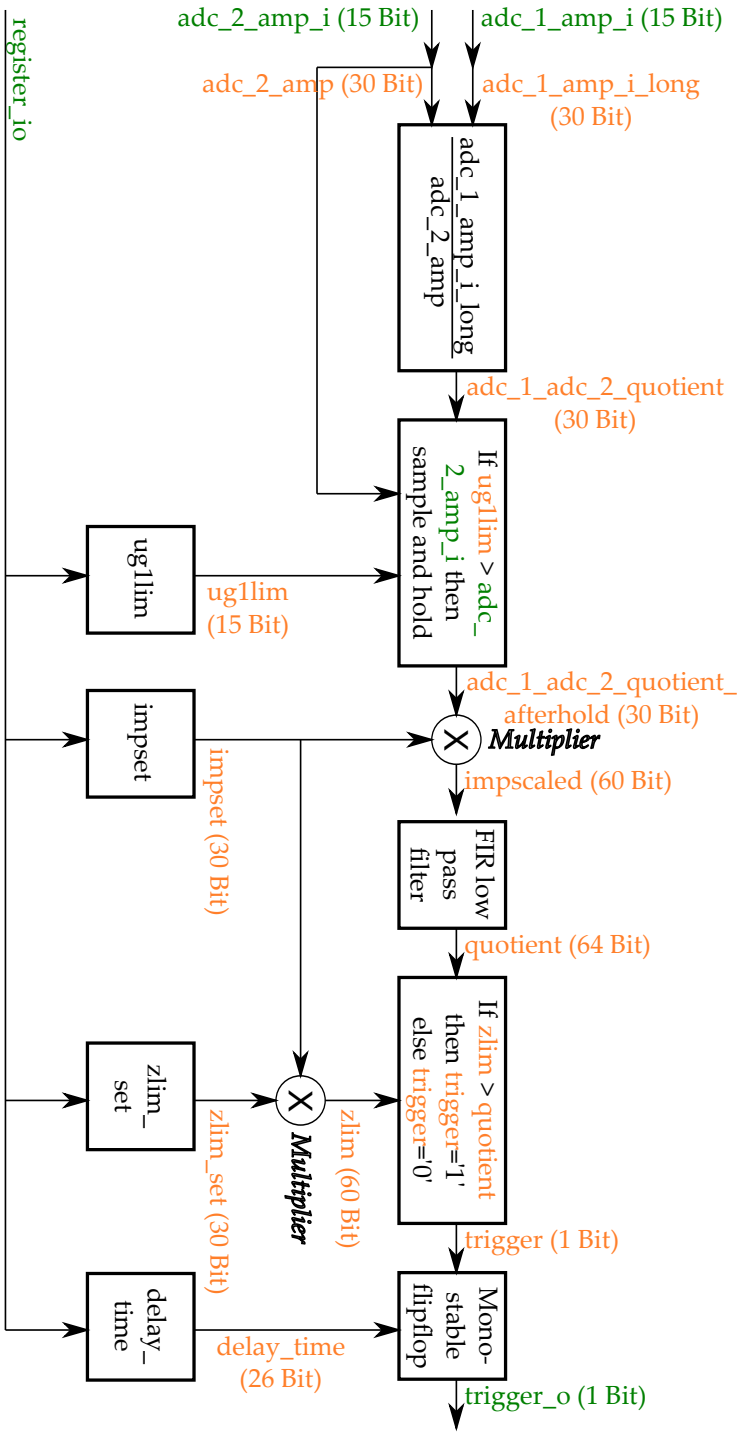

Figure 5.3: *Schematic of the arc detector core: Ports are illustrated in green, signals in orange.*

5.2.3 Development and Simulation of the Detector Framework and the Arc Detector Core

In order to develop and optimize the coded algorithm, the simulation software ModelSim 6.6d by MentorGraphics has been used. Therefore a test bench was programmed, in which the algorithm was tested under several different conditions regarding the input signals.
One simulation has been made to verify the amplitude detection. For both ADC1 and ADC2 a 5 MHz sine with the maximal possible amplitude (equivalent to 1 Vp input voltage) was simulated as input signals. Figure 5.4 shows the plots of the reset signal, ADC1 and ADC2 signals as well as the ADC1 and ADC2–amplitude signals of the amplitude and phase–detector package.

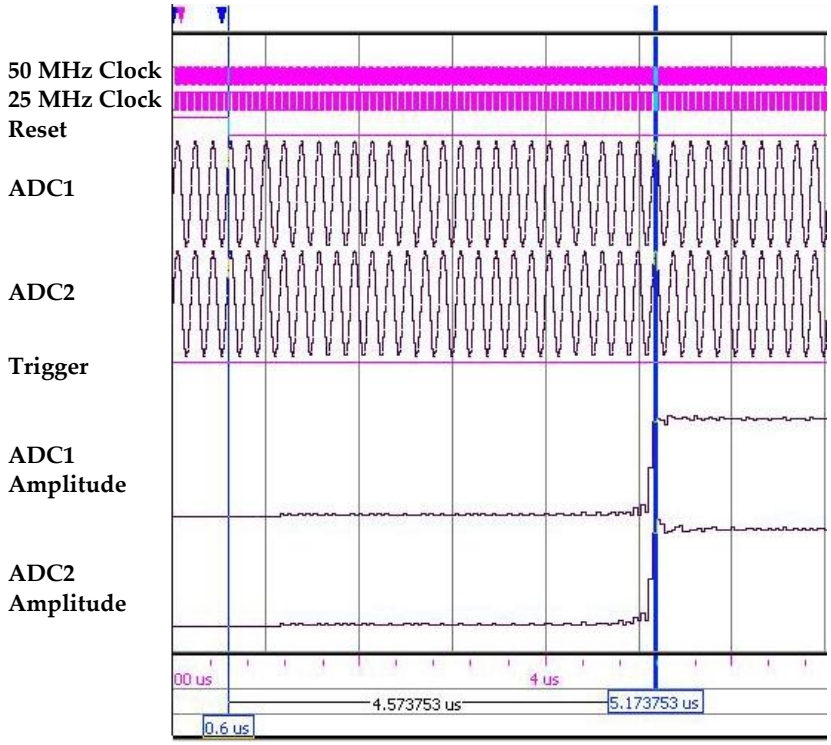

Figure 5.4: *Simulation of detector framework and arc detector core without triggering: From top to bottom the signals of the 50 MHz clock, the 25 MHz clock, the reset, the ADC1, the ADC2, the trigger, the ADC1 amplitude and the ADC2 amplitude are plotted. The blue vertical lines are indicating cursor positions for time measurement.*

The amplitude signals need time to rise to the maximal value. This simulated amplitude response time was determined by using the cursor function in the simulation software. The cursors were positioned on the falling edge of the reset signal and the point of time when the amplitude signals are reaching 90 % of their full amplitude. This yields 4.57 ± 0.01 μs for the simulated amplitude response time for both ADC channels.
Another simulation was made to test the triggering. Therefore again both ADC signals have been set to 5 MHz and to the maximal possible amplitude. After 70 cycles the ADC1 signal was set to zero. This behavior occurs in an idealized case of an electric arc inside the cavity. Figure 5.5 shows the plots of the signal of the ADC1 signal, the trigger signal and the ADC1–amplitude signal of the amplitude and phase–detector package.
At a simulation time of 13.30 ± 0.01 μs it can clearly be seen that the ADC1 signal is set to zero. After 4.61 ± 0.01 μs the amplitude signal of ADC1 is starting to fall, and another 0.30 ± 0.01 μs later the trigger signal is sent out. This yields a simulated trigger response time of 4.91 ± 0.01 μs.
It was also shown that the triggering is following exactly the set threshold. This was tested by downscaling the amplitude of ADC1 signal at a constant amplitude of the ADC2 signal until triggering at different preset thresholds.

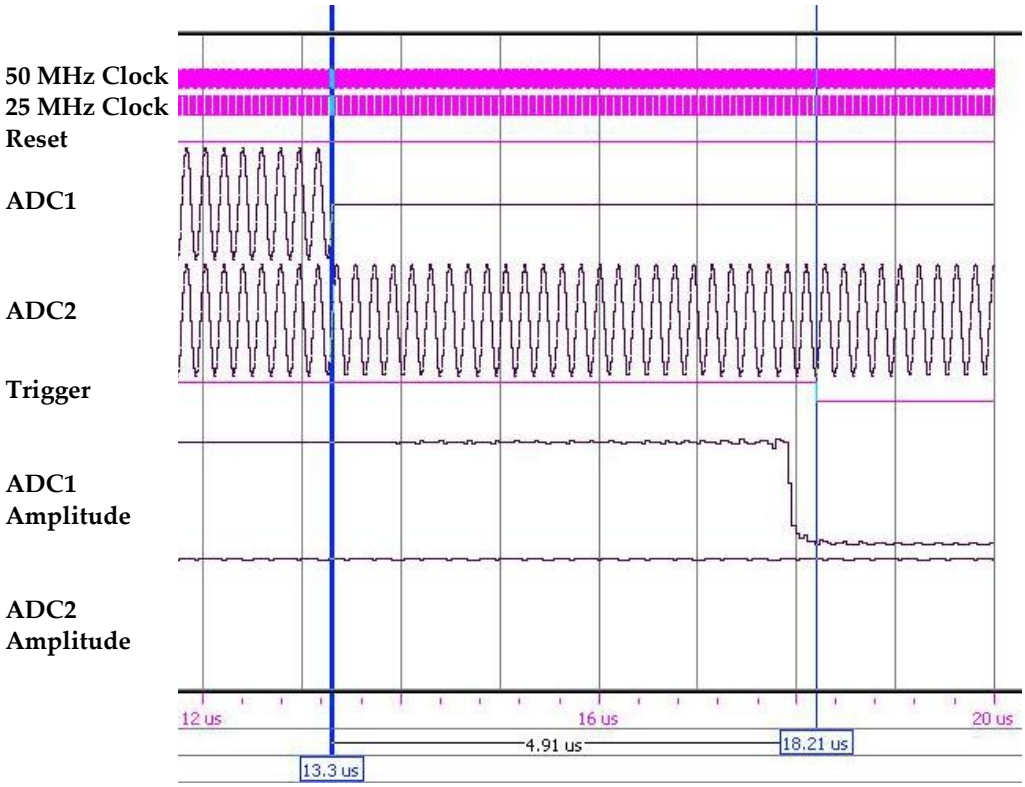

Figure 5.5: *Simulation of detector framework and arc detector core with triggering: From top to bottom the signals of the 50 MHz clock, the 25 MHz clock, the reset, the ADC1, the ADC2, the trigger, the ADC1 amplitude and the ADC2 amplitude are plotted. The blue vertical lines are indicating cursor positions.*

5.2.4 FPGA Universal Bus

The FPGA Universal Bus is a norm developed by the RF group at GSI for the internal communication interface between packages on FPGAs. Beside a data and an address signal it provides also a handshake. There are two possible structures [18].
The first possibility is that the transmitter is master and the receiver is slave. In this case the transmitter sends while sending an 8–bit data vector and an 8–bit address vector a 1–bit strobe signal to the receiver. The strobe signal validates the data and address sent. If there the strobe signal is low, the receiver ignores the incoming data and address. Delayed by one clock cycle the receiver returns a 1–bit busy signal to the transmitter as long as the

data are processed. With this configuration the writing of data to a certain address from the transmitter package to the receiver package can be realized. The second possibility is that the transmitter is slave and the receiver is master. In this case the receiver sends in addition to an 8–bit address vector an 1–bit strobe signal to validate the address. One clock cycle later the transmitter sends an 8–bit data vector and an 1-bit busy signal to the receiver. The data sent in the data vector has been read from the address that was sent by the transmitter. This configuration can be used to realize a read process at a certain address at the transmitter package initiated by the receiver package.

5.3 Software Configuration of the FIB–FAB

As described in chapter 3 the arc detector has to be configurable in such a way that the threshold, the nominal gap voltage amplitude, and the nominal grid–1 voltage amplitude can be set. The interface for the configuration is the RS–232 interface on the FAB.
The configuration data that is sent to the FPGA consists of two bytes of address information, one byte of data and one byte for the checksum. Instead of using the software HTerm with a hexadecimal sequence as input, RFDevConf is used, which was developed at the RF group at GSI. It is programmed in Qt and can be configured by .xml files. Figure 5.6 shows the main menu of the application.

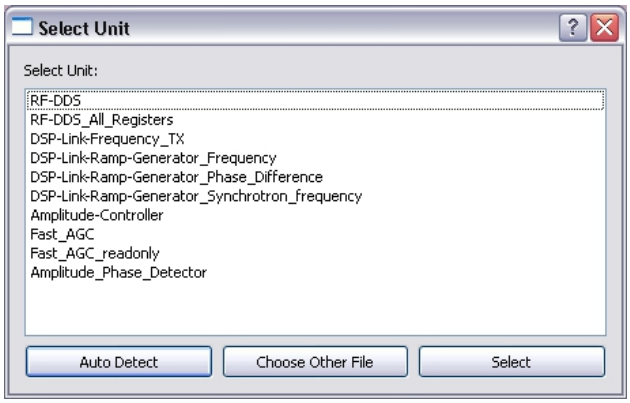

Figure 5.6: *RFDevConf main menu consisting of a list of selectable units.*

To realize the configurability of the arc detector a new .xml configuration file for RFDefConf was written. Figure 5.7 shows the configuration menu for

the arc detector. It provides drop–down menus for the blocked–out interval, the impedance of the cavity, the impedance threshold, and the trigger–hold time (cf. chapter 5.2.2) as well as input boxes for the ADC1 and ADC2 amplitude scale factor and the ADC1 and ADC2 offset value with drop down menus to set the respective sign (cf. chapter 5.2.1). Below this there are two buttons for reading and writing the RAM. All values shown are default values of the configuration of the arc detector.

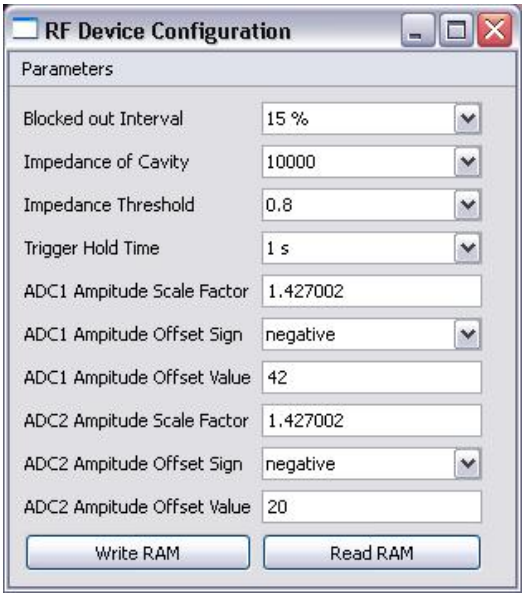

Figure 5.7: *RFDevConf Arc Detector Configuration Menu consisting of drop–down menus for the blocked–out interval, the impedance of the cavity, the impedance threshold, and the trigger hold time as well as input boxes for the ADC1 and ADC2 amplitude scale factor and the ADC1 and ADC2 offset value with drop down menus to set the respective sign. Below this there are two buttons for reading and writing the RAM.*

5.4 Assembly

After the implementation of the algorithm for arc detection, a front panel for the final assembly has been designed. The hardware of FIB and FAB is mounted in an RF housing so that the device can be operated within a standard 19–inch rack.
In the future the functionality of the arc detector and the full functionality of the amplitude and phase detector [12] will be unified in one device. Thus

the front panel of the arc detector is the same as the one of the amplitude and phase detector. Figure 5.8 shows a picture of the assembled arc detector.

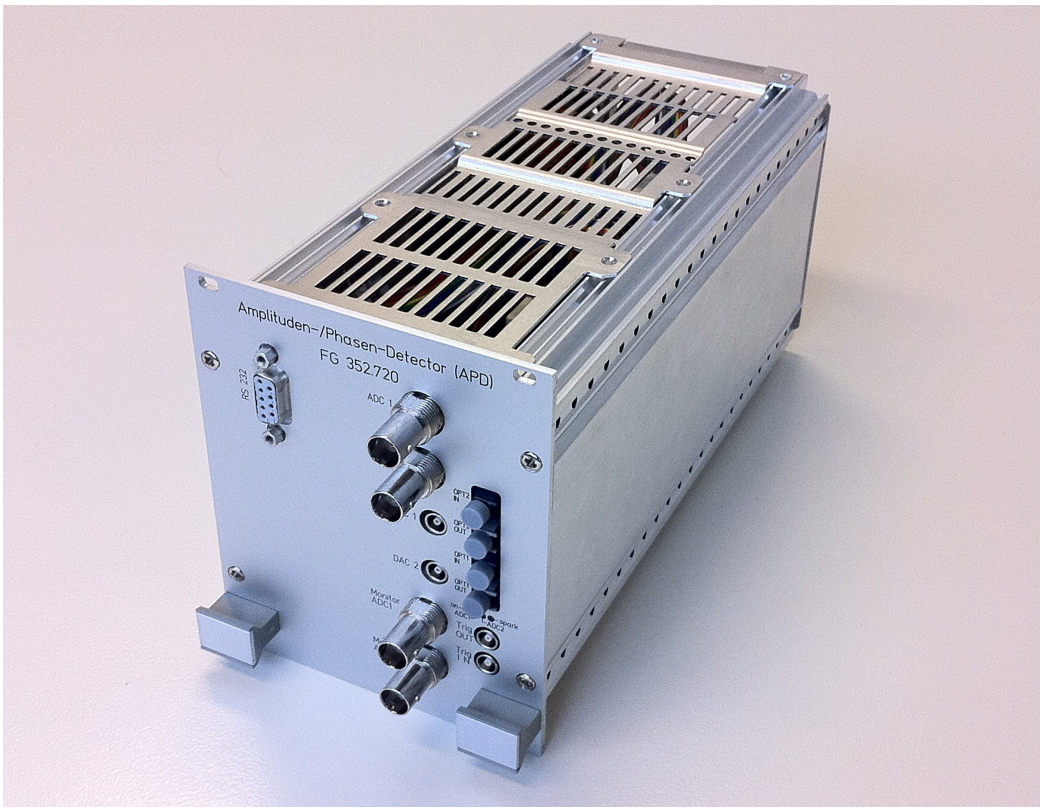

Figure 5.8: *Arc Detector: In the upper left corner of the front panel the RS–232 interface is located. In the middle column from top to bottom there are the BNC input plugs for the ADC1 and ADC2 channels, the LEMO output plugs for DAC1 and DAC2 as well as the BNC output plugs for ADC1 and ADC2 monitoring. In the right column from top to bottom there are two optical input and two optical output interfaces, four LEDs indicating that the arc detector is working, incoming signals for ADC1 and ADC2 as well as the detection of an arc, the LEMO plug for the trigger output signal and a LEMO plug for a trigger input signal. The front panel has a width of 10.6 cm and a height of 12.85 cm.*

Chapter 6

Verification of Functionality within a Test Environment

After the design, development, and assembly of the arc detector its functionality and performance has been tested in a test environment. In figure 6.1 the setup is shown.
The analysis was split into two steps. First the characteristics of the amplitude detection for both ADC1 and ADC2 channel have been measured (cf. chapter 6.1). Secondly the characteristics of the triggering have been measured (cf. chapter 6.2).

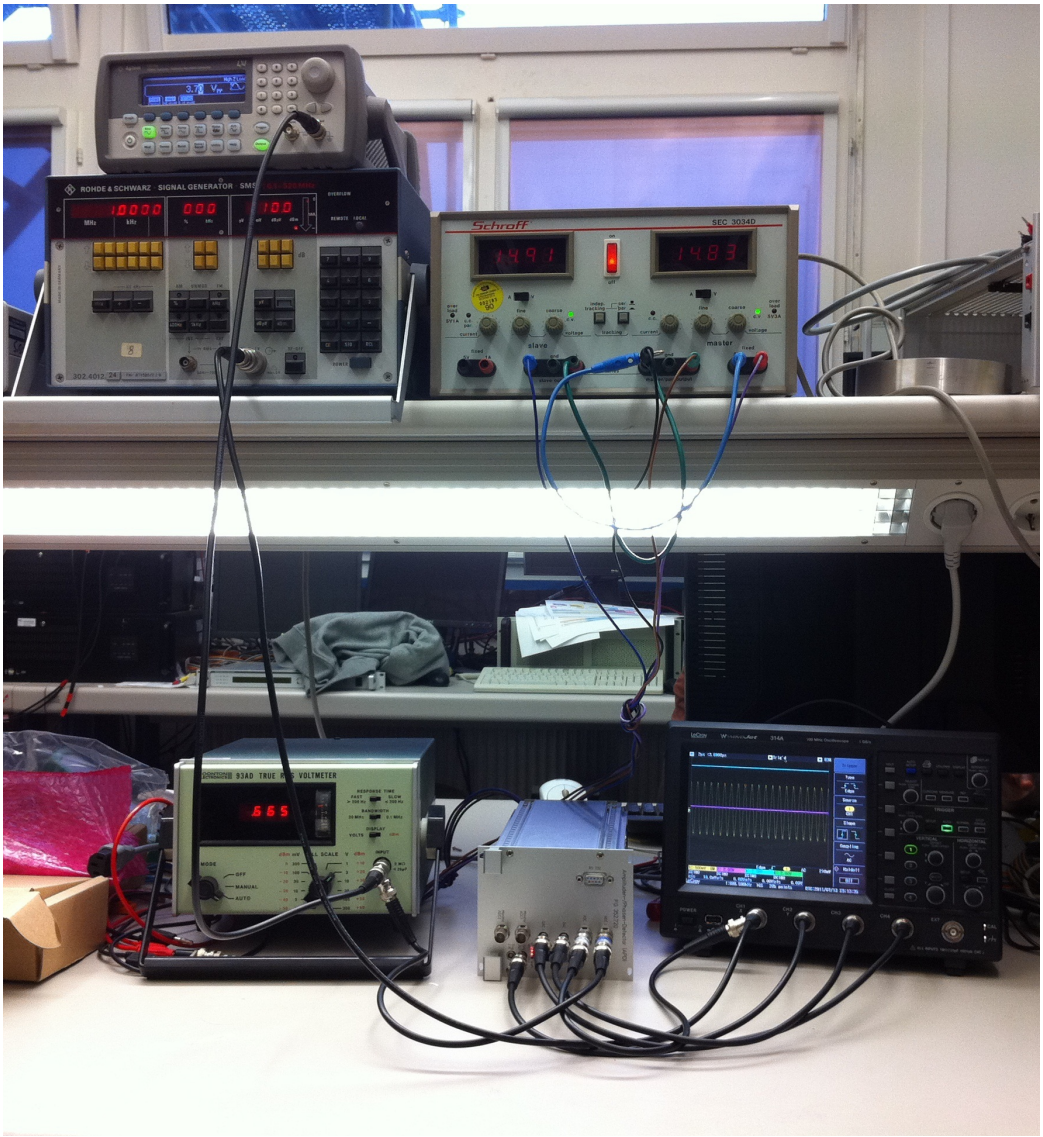

Figure 6.1: *Picture of the Test Setup: On the left hand side of the shelf two arbitrary waveform generator are located. In the right hand side of the shelf there is the voltage supply for the arc detector. On the left hand side on the table is the true RMS voltmeter, in the middle is the arc detector and on the right hand side is the oscilloscope located.*

6.1 Characteristics of Amplitude Detection

In order to measure the characteristics of the amplitude detection, the test setup shown in figure 6.2 was used. Thereby the following devices and instruments have been utilized:

- Rohde & Schwarz Signal Generator SMS 0.1 - 520 MHz
- Boonton Electronics 93AD True RMS Voltmeter
- Hewlett Packard 34401 A Multimeter

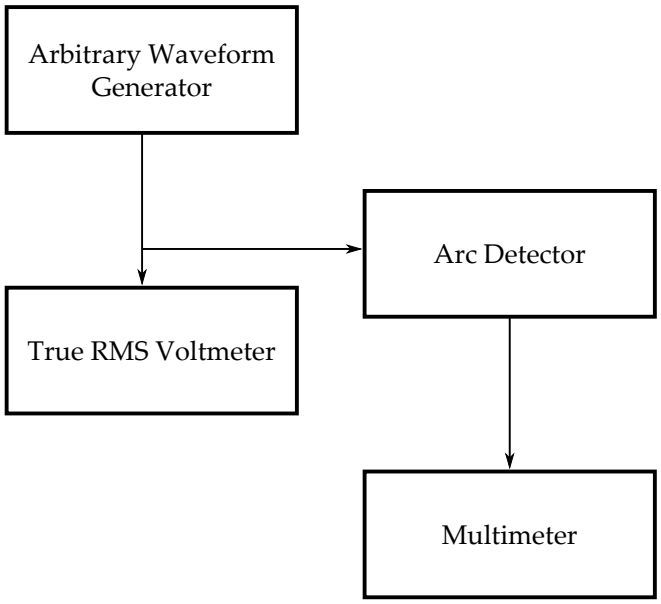

Figure 6.2: *Schematic of the test setup for measurements of characteristics of amplitude detection: The RF signal generated by the arbitrary waveform generator is detected by a true RMS voltmeter and the arc detector. The amplitude signal generated by the arc detector is measured by a multimeter.*

An RF signal with an arbitrary amplitude and frequency was generated by an arbitrary waveform generator (AWG). To determine the reference amplitude of this signal, a true RMS voltmeter was used. The RF signal was also sent to the arc detector. The amplitude signal produced by the detector was monitored on a multimeter.

Using this configuration the amplitude output signal of the arc detector depending on different combinations of input amplitudes (0 to 1 Vp) and frequencies (0.4 to 6 MHz) was measured. This was separately done for both the ADC1 and ADC2 channels. Figure 6.3 shows a 3D plot of the recorded data for the ADC1 channel. The respective values are listed in tables A.1 to A.7 in appendix A. Figure 6.4 shows the data for the ADC2 channel. The values are listed in tables A.8 to A.14 in appendix A.

Both plots show a linear dependency between input and output voltages with a noise floor at low input voltages and a frequency dependency, clearly to see at high input voltages. This characteristics are quantized in the following chapters 6.1.1 and 6.1.2.

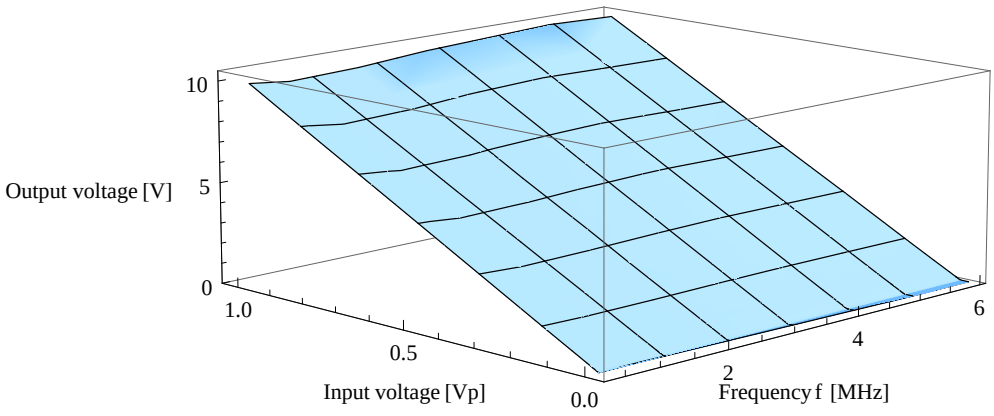

Figure 6.3: *Measured values of ADC1 channel: Plotted is the output voltage as a function of the voltage and the frequency.*

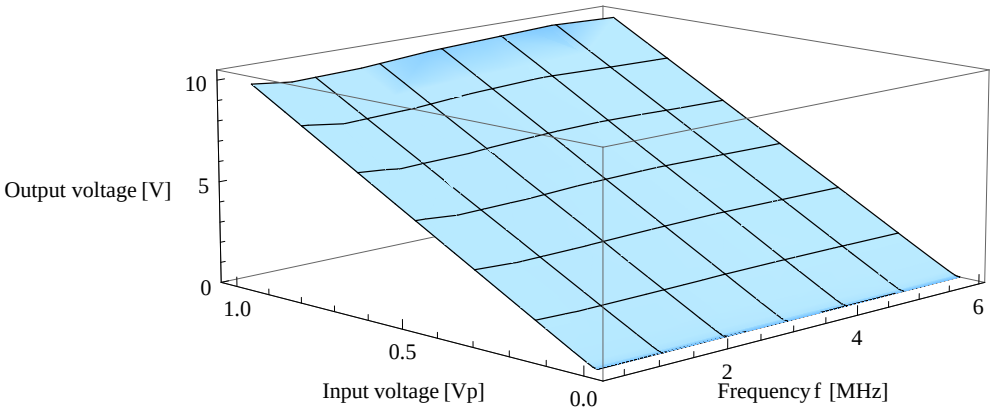

Figure 6.4: *Measured values of ADC2 channel: Plotted is the output voltage as a function of the voltage and the frequency.*

6.1.1 Linearity

To characterize the linearity of the two channels of the arc detector, the amplitude output signal depending on the input RF signal was measured for several different frequencies. Figures 6.5 and 6.6 show projections of figures 6.3 and 6.4 on the x–y–plane.
In order to analyze the noise floor at low input voltages and the linearity, the ratio between output and input signal was computed. Figures 6.7 and 6.8 show the ratios for both channels. The amplitude detection was designed that the amplitude output signal is linear proportional to the amplitude of the RF input signal and is ten times its half amplitude. Thus the theoretical ratio of input and output signal is 10. Both figures show that this is valid for the actual values for both channels of the arc detector except for low input voltages.
With an allowed variation of 3% of the ratio [12] this yields a dynamic of 47.3 ± 0.1 dB for the ADC1 channel and 36.4 ± 0.1 dB for the ADC2 channel. This would not fulfill the specifications of the amplitude detector of 60 dB [12, 10] but it is highly sufficient for the arc detector, due to the default masking of 15% of the maximal input amplitude (cf. chapter 5.2.2), which yields the required dynamic range of 16.5 dB.

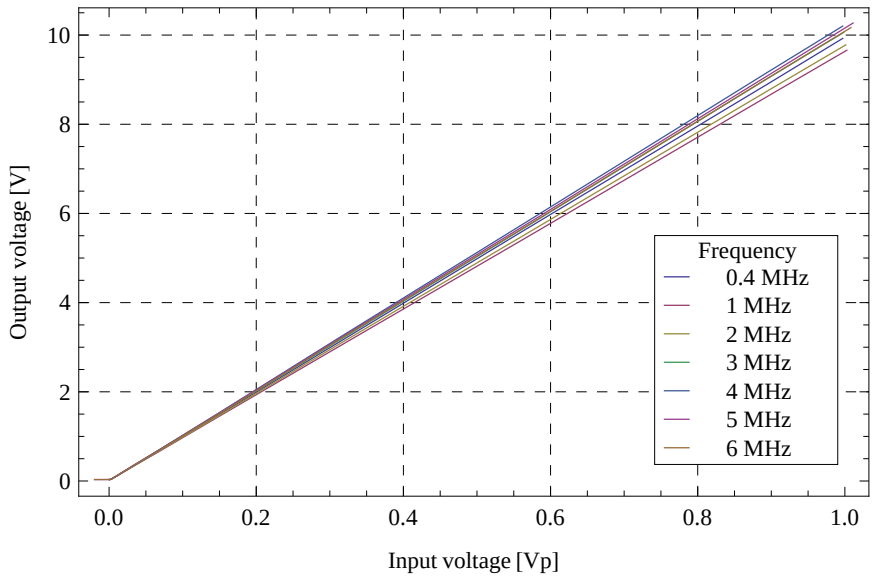

Figure 6.5: *Linearity of ADC1 channel: Output voltage over input voltage measured at several frequencies.*

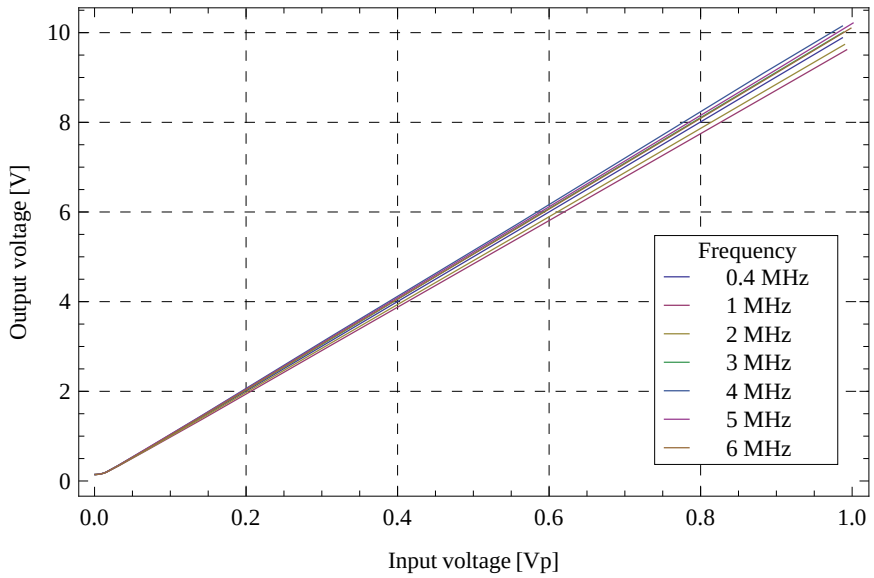

Figure 6.6: *Linearity of ADC2 channel: Output voltage over input voltage measured at several frequencies.*

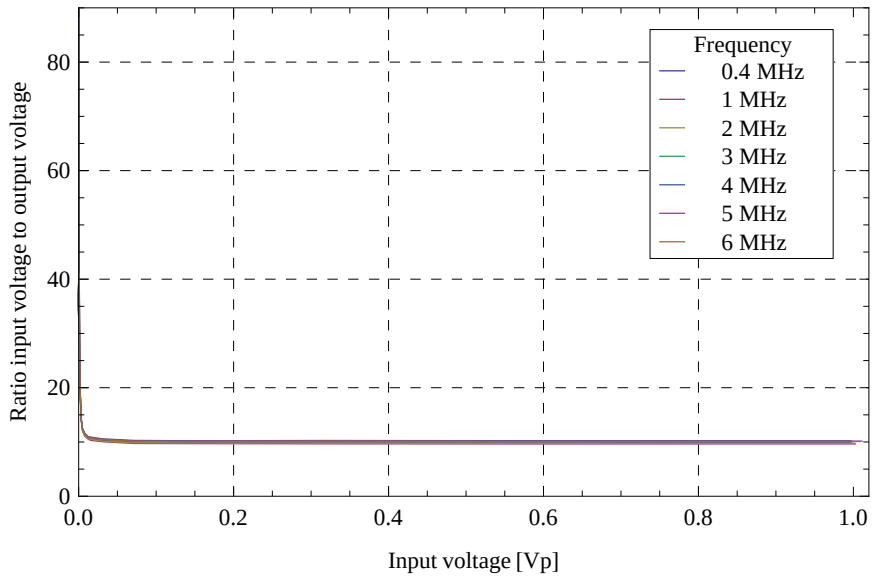

Figure 6.7: *Ratio of input to output signal for the ADC1 channel as a function of input voltage.*

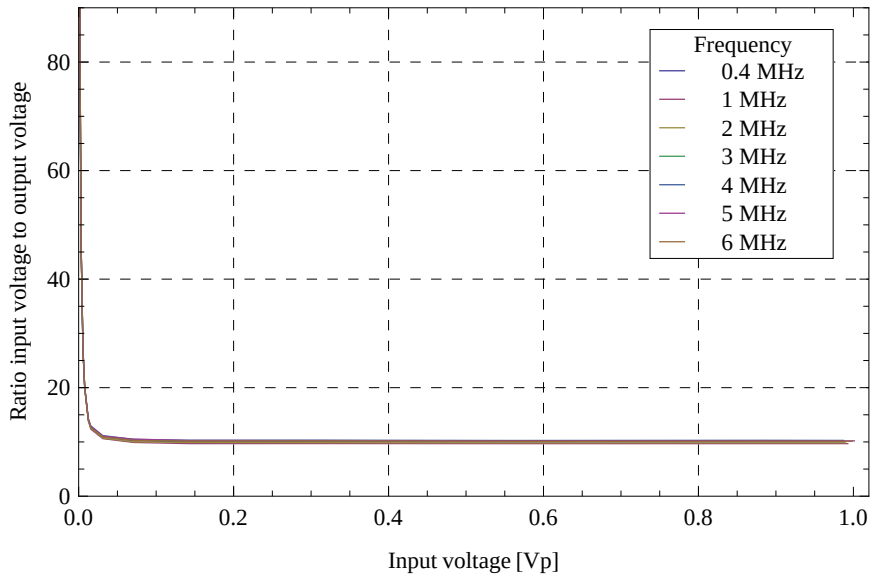

Figure 6.8: *Ratio of input to output signal for the ADC2 channel as a function of input voltage.*

6.1.2 Frequency Dependency

In figures 6.3 to 6.6 a frequency dependency of the measurement is observed. Hence figures 6.9 and 6.10 show the respective output voltage of the ADC1 and ADC2 channel as a function of the frequency.
One finds a weak frequency dependence with a minimum at about 1 MHz and a maximum at about 5 MHz. For both the ADC1 and ADC2 channel the variation is up to 6%. This fits exactly the requirements of the amplitude detector of 6% defined in [10].
In the case of the arc detector the ratio of the amplitudes of the ADC1 and ADC2 input signal is computed (cf. chapters 1.5.2 and 5.2.1). Figure 6.11 shows the frequency dependence of the ratio of the gap voltage and the grid–1 voltage of the tetrode. Because of the masking of 15% of the maximal amplitude (cf. chapter 5.2.2) only high input voltages from 0.997 Vp down to 0.143 Vp have been considered.

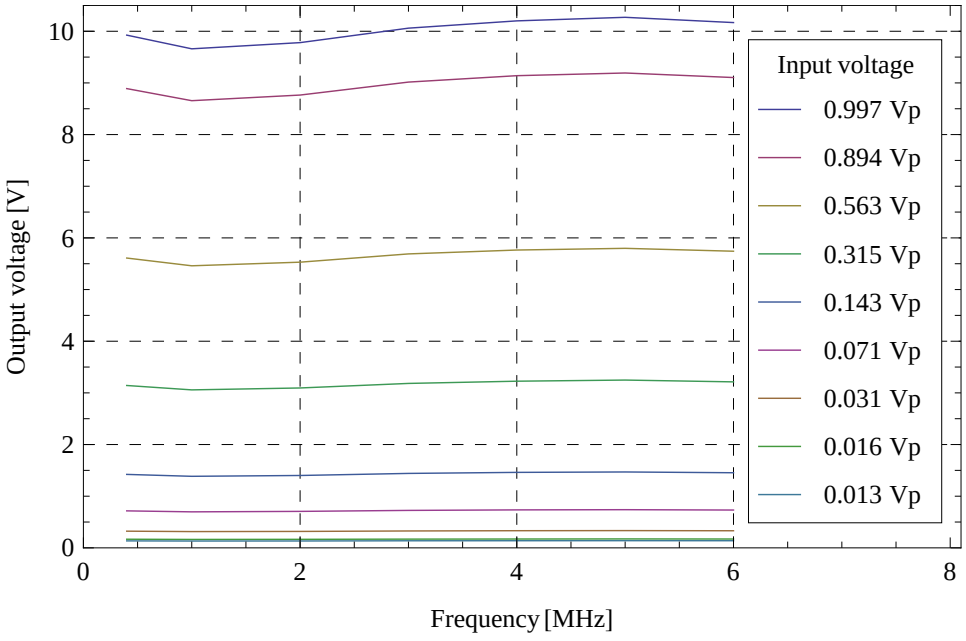

Figure 6.9: *Frequency dependency of ADC1 channel: Output voltage over frequency at several input voltages.*

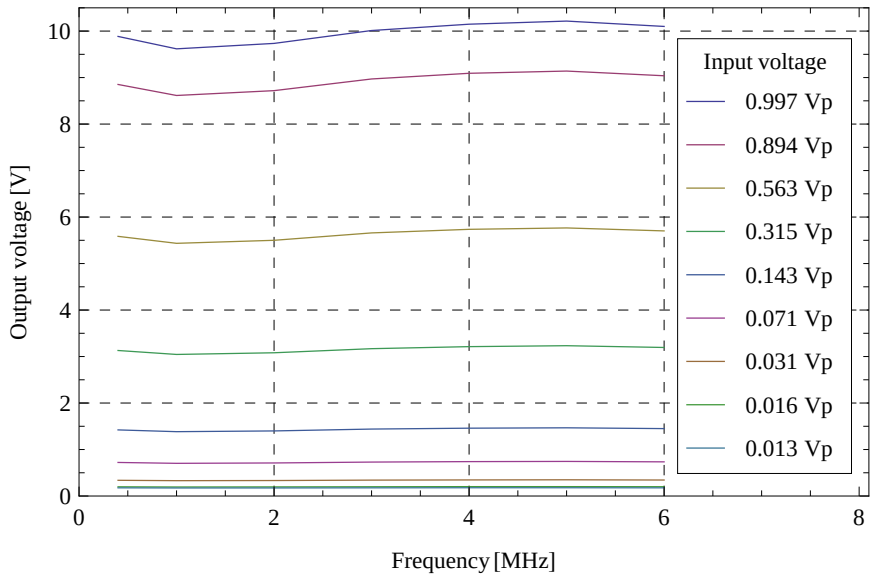

Figure 6.10: *Frequency dependency of ADC2 channel: Output voltage over frequency at several input voltages.*

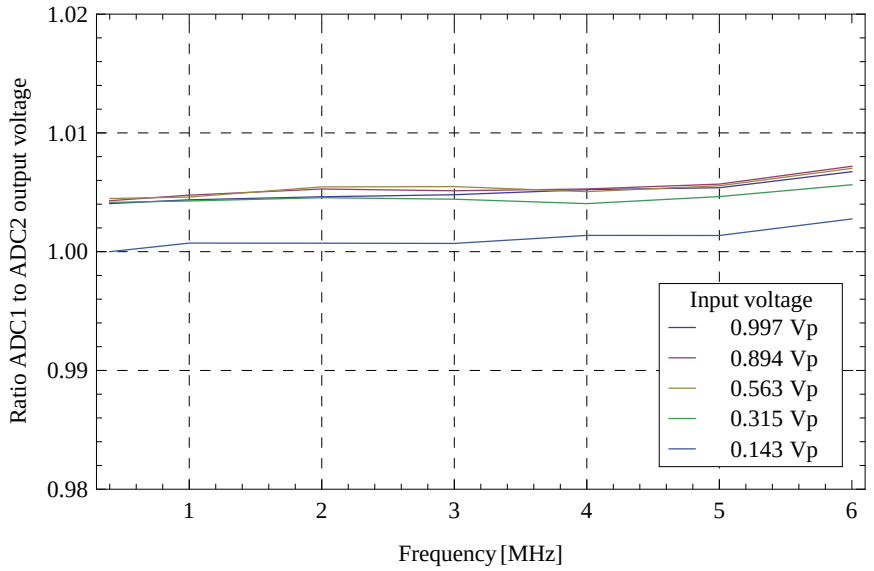

Figure 6.11: *Ratio of output voltages from the ADC1 and ADC2 channels as a function of frequency for several input voltages.*

The ratio of the frequency dependency of both channels is in average 1.005 for all input voltages and frequencies. The variation of the ratio is 0.3%. The characteristics of both channels are exactly the same and thus the frequency dependency can be neglected for the arc detection.

6.1.3 Amplitude Response Time

Another important characteristic of the amplitude detection is the response time of the amplitude output signal. The data that is sent to the respective DAC to generate the signal is also used for computation in the arc–detection algorithm. Thus the amplitude response time has an influence on the trigger response time (cf. chapter 6.2.2) for the arc detection.
In order to determine the amplitude response time, the test setup shown in figure 6.12 was used. A burst with 500 cycles of an RF signal with a frequency of 1 MHz and an amplitude of 1 Vp was generated by an AWG and sent for detection to the arc detector and for monitoring and measuring to an oscilloscope. At the same time the amplitude output signal of the arc detector was measured with the oscilloscope. The amplitude response time that has been determined is the time from the beginning of the burst to 90% of the amplitude output signal.

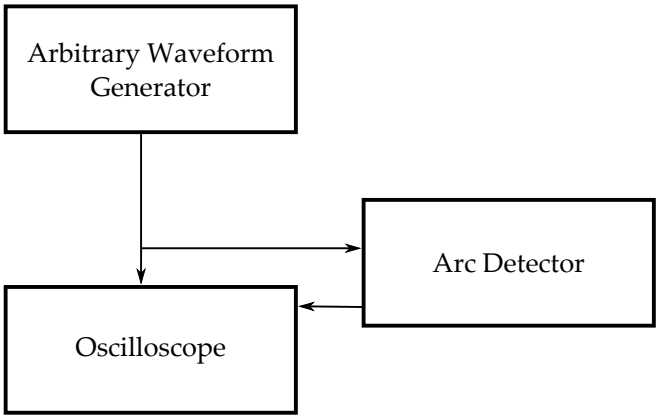

Figure 6.12: *Schematic drawing of the test setup for measuring the rise time for the amplitude detection: The RF signal generated by the arbitrary waveform generator is detected by the oscilloscope and the arc detector. The amplitude output signal of the arc detector is also measured by the oscilloscope.*

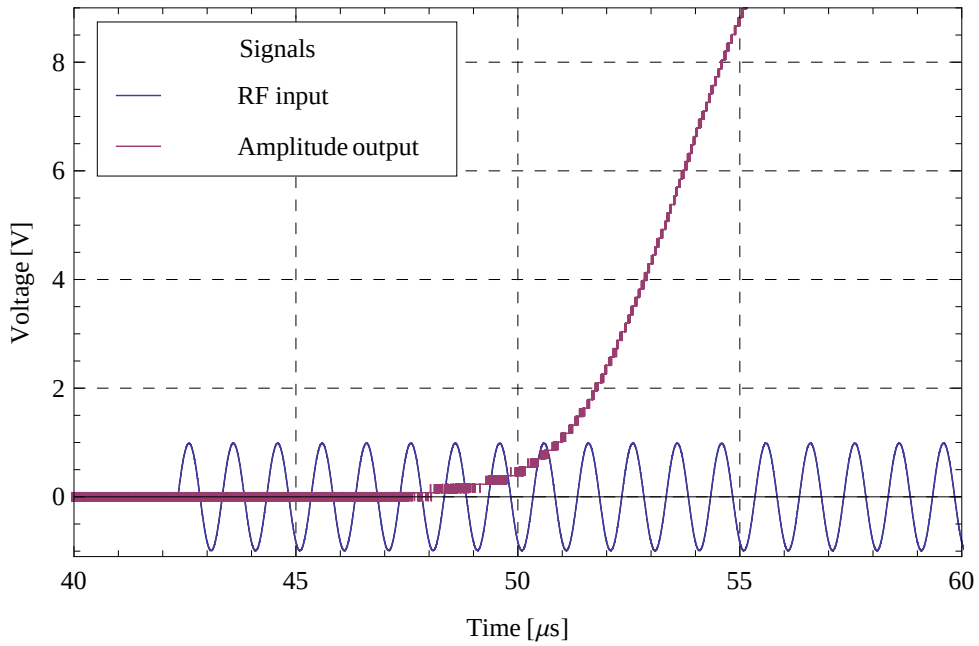

Figure 6.13: *Measurement of the amplitude response time for the example of the ADC1 Channel: The output voltage is displayed as a function of time.*

This measurement was done for ADC1 and ADC2 separately. Figure 6.13 shows the measurement for ADC1. Choosing the maximal possible amplitude for the input signal yields the longest possible rise times. They amount to 12.85 ± 0.01 μs for the ADC1 channel and 12.64 ± 0.01 μs for the ADC2 channel.

6.2 Characteristics of Triggering

In order to quantify the characteristics of triggering, a test setup according to figure 6.14 was used. The following devices and instruments have been used:

- Agilent 33210A Function / Arbitrary Waveform Generator 10 MHz
- Rohde & Schwarz Signal Generator SMS 0.1 - 520 MHz
- LeCroy WaveJet 324A Oscilloscope

Two arbitrary waveform generators generated the input signals for the arc detector. These were also measured by the oscilloscope. One AWG

emulated the RF signal of the grid–1 voltage of the tetrode and the other the RF signal of the gap voltage of the cavity. Both the characterization of the actual trigger threshold and of the trigger response time have been done by using the described test setup.

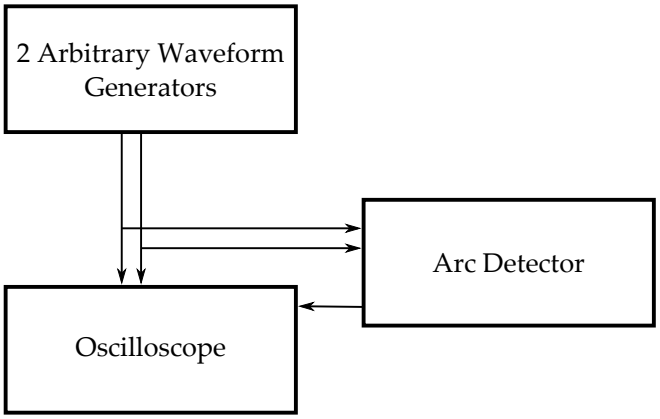

Figure 6.14: *Schematic of the test setup for measuring the characteristics of triggering: Two RF signals generated by arbitrary waveform generators are detected by the oscilloscope and the arc detector. At the same time the trigger output signal of the arc detector is measured by the oscilloscope.*

6.2.1 Actual Trigger Threshold

In the following the relation between the set value for the triggering and the actual value is examined. Therefore a test setup as shown in figure 6.14 was used. The input signal for the ADC2 channel, which detects the grid–1 voltage of the tetrode, was a 1 MHz RF signal with an amplitude of 0.99 Vp. At the beginning of the measurement the same signal was also used as an input signal for the ADC1 channel, which is detecting the gap voltage of the cavity. After the trigger threshold was set using RFDevConf the amplitude of the input voltage of the ADC1 channel was lowered until the arc detector sent out a trigger signal.
The results of the measurement is listed in table A.15 in appendix A and is plotted in figure 6.15. The actual trigger threshold is 4.7 % higher in average then the set threshold with a standard deviation of 0.4 %. This is due to the different scaling factors set for the ADC1 and ADC2 channel with a difference of 4.5 % in order to maximize the dynamic range of both channels separately.

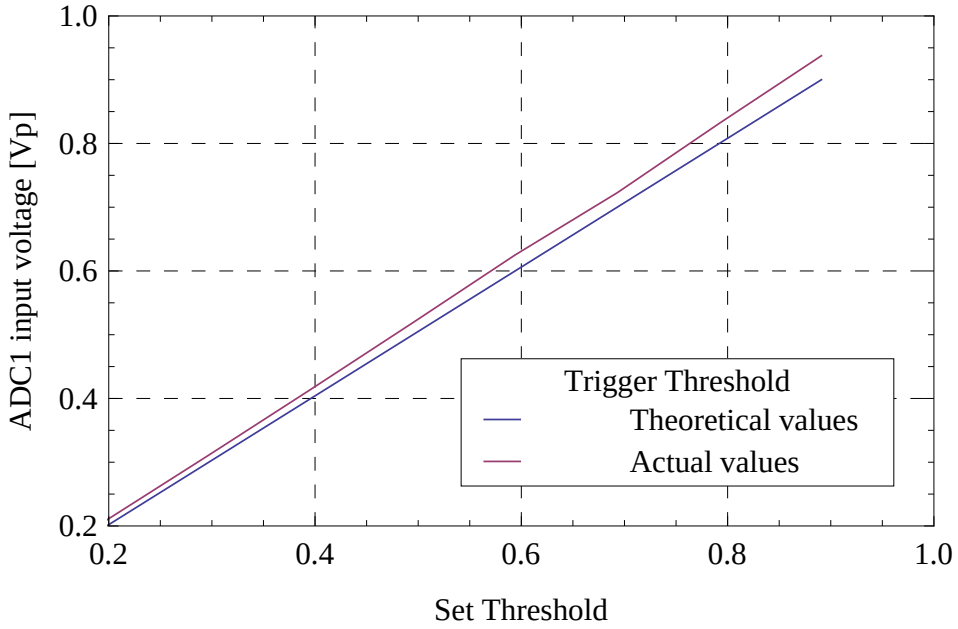

Figure 6.15: *Trigger threshold: ADC1 input voltage over theoretical and actual threshold.*

6.2.2 Trigger Response Time

The trigger response time is the time the arc detector needs from a trigger event until the full rise of the trigger signal output. For determining this time the test setup described in figure 6.14 was used. Two AWGs sent an RF signal with a voltage of 0.99 Vp at frequency of 1 MHz each to the ADC1 and ADC2 channels of the arc detector and for monitoring purpose to the oscilloscope. An electric arc was emulated by switching off the input signal for the ADC1 channel. At the same time the trigger signal of the arc detector was measured. The trigger threshold was set to the default value of 0.8. Figure 6.16 shows the outcome of the measurement.
In this case the most pessimistic time for the trigger response time was determined, namely from the last maximum of the RF input signal at the full amplitude to the full rise of the trigger signal. This yields a trigger response time of 7.8 ± 0.1 μs, which is about two orders of magnitude shorter than the requirement of 1 ms required as listed in table 3.1.

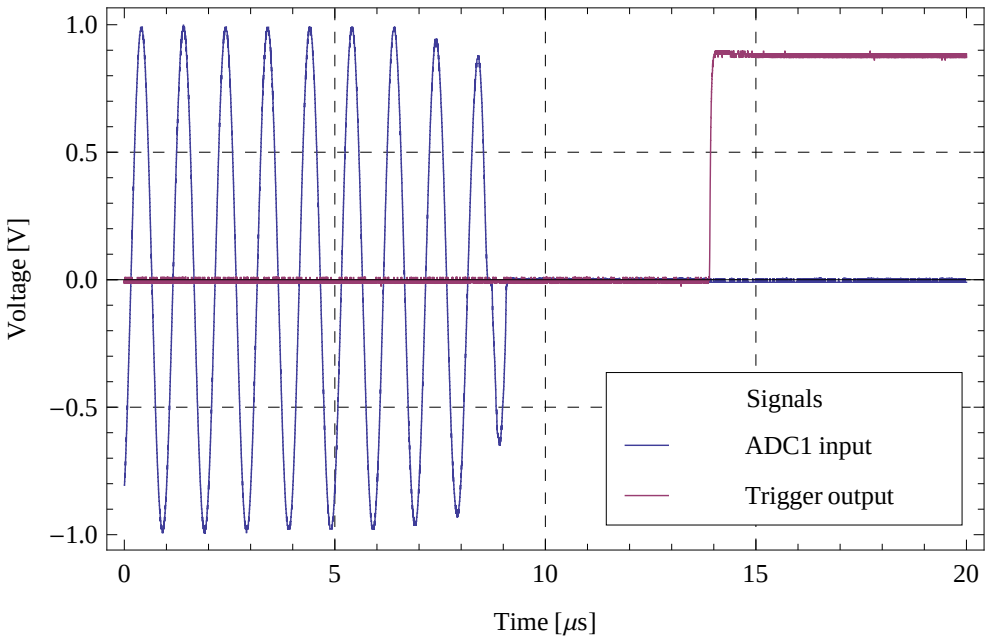

Figure 6.16: *Trigger response time: Emulated gap–voltage signal and trigger signal as a function of time. The output trigger signal has been scaled down by the factor of 5 for better visibility.*

6.3 Overview of the Test Readings

Table 6.1 lists an overview of the experimental test readings in comparison to the simulated values and the requirements. All requirements for the arc detector have been fulfilled by the present design, which means a verification of its functionality in the test environment.
The simulated values for the amplitude response times for the ADC1 and ADC2 channels as well as the trigger response time are shorter than the actual values. This is due the fact that the simulation software does not take processing times on the FPGA into account. In reality there is a run duration for every logic element on the chip. In addition in the case of the amplitude detection the time needed for the analog signal processing by an operational amplifier and a reconstruction filter in the DAC channel is not taken in account in the simulation.

Parameter	Required values	Simulated values	Measured values
Dynamic range of ADC1 channel (cf. chapter 6.1.1)	16.5 dB (60 dB)		47.3 ± 0.1 dB
Dynamic range of ADC2 channel (cf. chapter 6.1.1)	16.5 dB (60 dB)		36.4 ± 0.1 dB
Variation of frequency dependency of ADC1 channel (cf. chapter 6.1.2)	6 % (6 %)		6 %
Variation of frequency dependency of ADC2 channel (cf. chapter 6.1.2)	6 % (6 %)		6 %
Ratio of frequency response ADC1 to ADC2 channel (cf. chapter 6.1.2)			1.005 ±0.3%
Amplitude response time ADC1 channel (cf. chapter 6.1.3)		4.57 ±0.01 μs	12.85 ±0.01 μs
Amplitude response time ADC2 channel (cf. chapter 6.1.3)		4.57 ±0.01 μs	12.64 ±0.01 μs
Variation actual to theoretical trigger threshold (cf. chapter 6.2.1)			4.7 % with $\sigma = 0.4$ %
Trigger response time (cf. chapter 6.2.2)	1 ms	4.91 ±0.01 μs	7.8 ±0.1 μs

Table 6.1: *Overview of the test readings: Parameters, required values, simulated values and measured values for the arc detector and in parentheses for the amplitude detector.*

Chapter 7

Application in a SIS–18 Prototype Cavity

7.1 Measurement Setup

The application of the arc detector in a SIS 18 prototype cavity aims on testing its functionality in a realistic environment including a real cavity, a realistic signal conduction, and influence of typical interference. The characteristics of arc detection are analyzed and quantized at constant and varying frequencies and amplitudes of the grid–1 and gap voltages. A schematic of the setup is shown in figure 7.1.

On one PC a set value for a frequency ramp was produced by the program milramp [19]. In order to define the shape of the ramp a list of data points representing frequency values from 800 kHz to 6 MHz at equidistant points of time was manually produced and loaded. By setting the sampling frequency the cycle time of the ramp was defined. The signal was sent to a MIL–Bus card [20] which generated a set signal of the frequency ramp for the control system.
On another PC a set value for an amplitude ramp was produced by the program AWGRampGen [21]. The software allows one to set the start delay time, the rise time, the flat top time, the fall time, the cycle time, the shape of the rising and falling edge, an offset and the amplitude of the amplitude ramp. The data is sent to an arbitrary waveform generator via a LAN (Local Area Network) connection. The start point of the cycle of the amplitude ramp was triggered on the falling edge of the frequency ramp.
The voltages of grid–1 of the tetrode and of the gap of the cavity were taped, divided down and sent to the arc detector. The scaling factor is $\frac{1}{200}$ for the

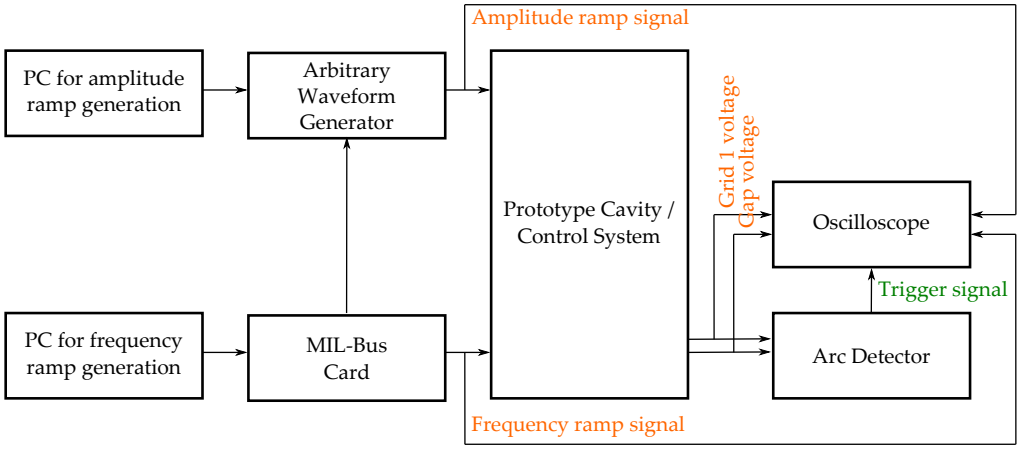

Figure 7.1: *Schematic of the setup involving the SIS–18 Prototype Cavity: Two PCs producing amplitude and frequency ramp set values and sending those to a MIL–Bus card and an arbitrary waveform generator, which are generating the set values for the control system of the prototype cavity. The amplitude ramp signal is triggered on the falling edge of the frequency ramp. The grid–1 and gap voltages are tapped, scaled down, and sent to the arc detector. The trigger signal of the arc detector as well as the grid–1 voltage, the gap voltage, the amplitude ramp signal, and the frequency ramp signal is monitored by an oscilloscope.*

grid–1 voltage and $\frac{1}{2000}$ for the gap voltage. Due to the fact that the final confirmation of application of the arc detector was not done yet the arc detector was not included in the control system of the cavity, but its output trigger signal was monitored by an oscilloscope instead. Also the scaled down grid–1 and gap voltages as well as the frequency ramp and the amplitude ramp signals were monitored with the oscilloscope. The arc detector was configured with RFDevConf. For all measurements the default configuration has been used. Figure 7.2 shows a picture of the measurement setup.

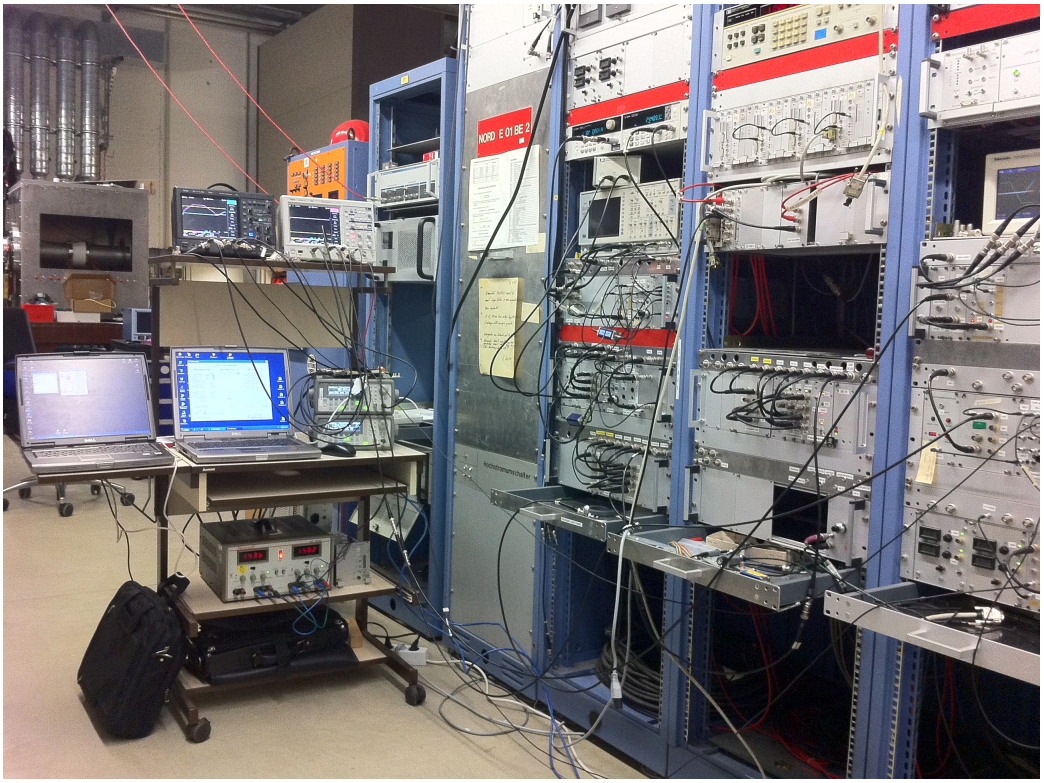

Figure 7.2: *Measurement Setup within the SIS 18 Prototype Cavity: On the left hand side from top to bottom: Two oscilloscopes for measuring the trigger signal of the arc detector, the scaled grid–1 and gap voltages, and the frequency and amplitude ramps; two PCs for configuring the arc detector and for creating a set signal for the amplitude ramp; two AWGs for generating the set signal of the amplitude ramp for the control system and for triggering the amplitude ramp; voltage supply for the arc detector. On the right hand side the control system of the SIS 18 prototype cavity can be seen.*

In order to produce electric arcs in the SIS 18 prototype cavity at low voltage amplitudes, the gap of the predetermined point of flashover was reduced to 0.5 mm. Figure 7.3 shows a picture of the respective area of the gap before the reduction of the gap distance.

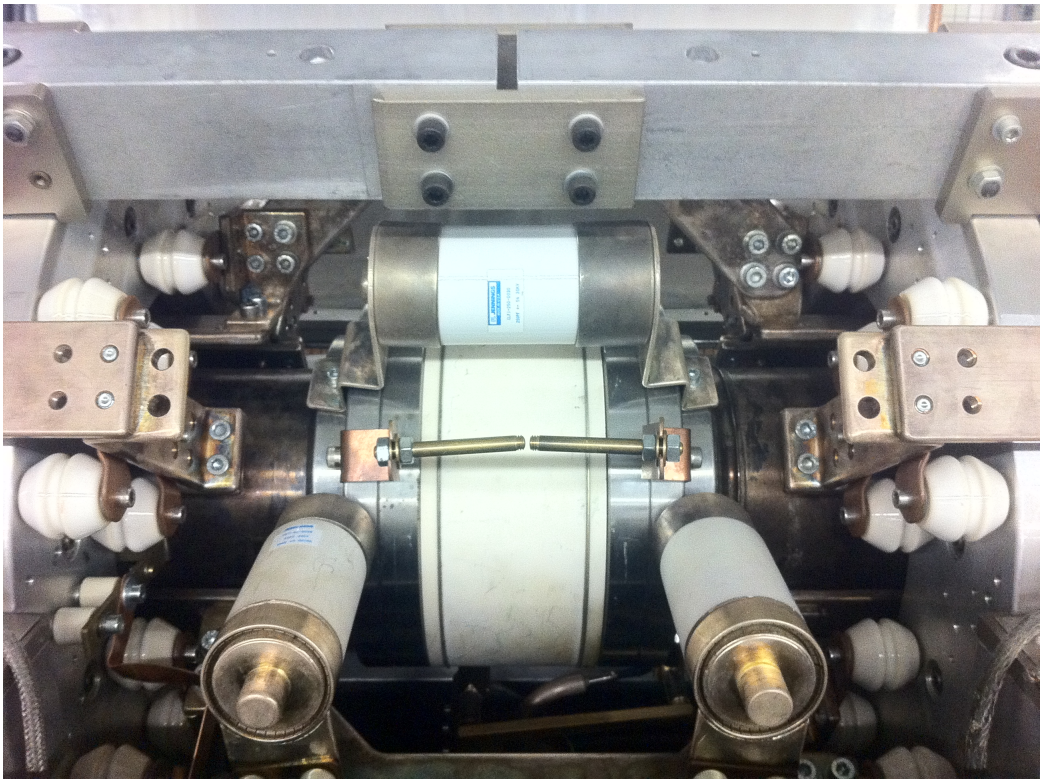

Figure 7.3: *Gap of the SIS 18 Prototype Cavity: In the middle there is the spark gap realized by two lances (gap distance 5 mm). Behind this there is the ceramic gap of the cavity in white dividing the beam pipe.*

7.2 Measurement at Constant Frequency

As a first step a continuous wave with a preset frequency of 3.24 MHz was generated inside the SIS 18 prototype cavity. The amplitude was manually slowly raised until an electric arc occurred inside the cavity. Figure 7.4 shows the scaled grid–1 voltage, the scaled gap voltage and the trigger signal of the arc detector.

The electric arc inside of the cavity occurred at a voltage amplitude of 1.656 ± 0.001 kV at the gap. The collapse of the gap voltage can be seen. About 5 μs later the grid–1 voltage rises. This is because the amplitude feedback control tries to compensate the missing voltage at the gap, which leads to an ongoing discharge. The trigger signal rises, too. The measurement of the trigger response time yielded 5.2 μs, i.e. 2.6 μs faster than in the idealized setup of chapter 6.2.2. This is due the fact that the amplitude

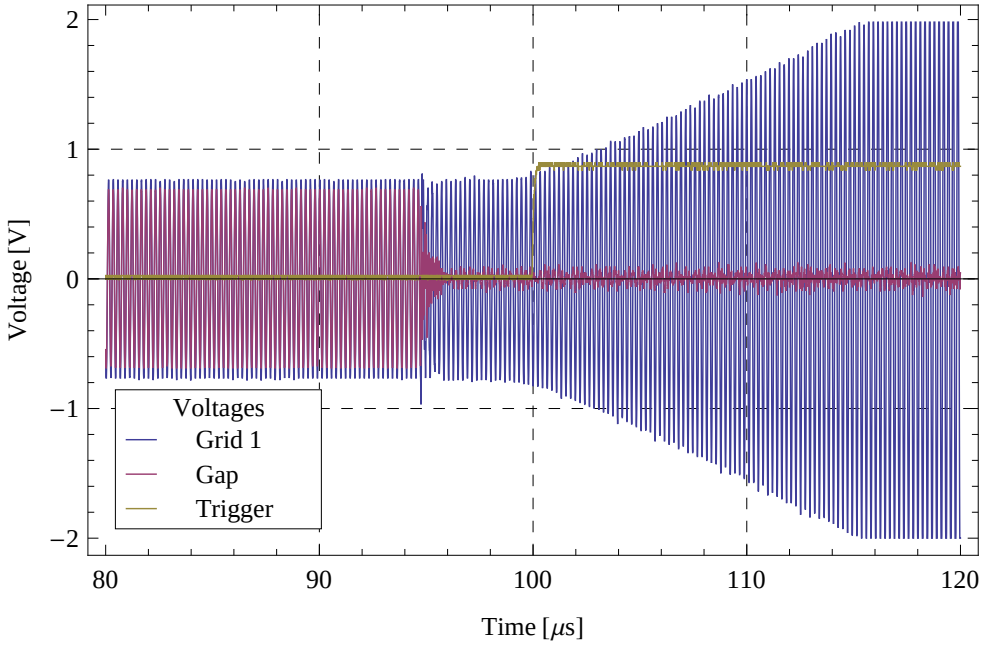

Figure 7.4: *Measurement of the trigger signal of the arc detector (divided by 5 for better visibility), the grid–1 voltage, and gap voltage at a continuous wave at 3.24 MHz and a slowly rising amplitude: Plotted is the respective voltage [V] over time [s].*

detected during the measurement within the prototype cavity was lower than in the test setup. A lower variation in amplitude results in a faster amplitude–response time, on which the trigger–response time depends on. Therewith a confirmation of application of the arc detector for the case of a constant frequency operation of the cavity was shown.

7.3 Realistic Acceleration Cycle with Frequency and Amplitude Ramps

As a second step the cavity was driven with a realistic acceleration cycle using frequency and amplitude ramps. For the amplitude ramp the start delay time was set to 100 ms, the rise time to 100 ms, the flap top time to 300 ms, the fall time to 100 ms, the cycle time to 1000 ms, and the amplitude to 0.5 kV. This amplitude was chosen to first run an acceleration cycle without an electric arc occurring. The rising and falling edge were set to be linear. For the frequency ramp rising and falling edges with no linear dependence on

time were chosen. The frequency range was set from 800 kHz to 6 MHz. Figure 7.5 shows the respective set signals, which were sent to the control system of the cavity.

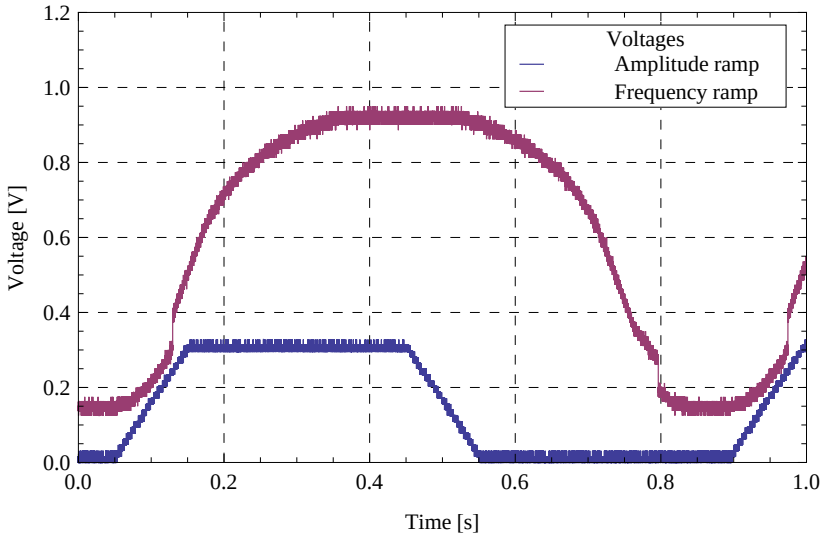

Figure 7.5: *Measurement of the frequency and amplitude ramp set signals.*

Figure 7.6 shows the trigger signal of the arc detector and the voltages of grid–1 as well as the gap for one acceleration cycle. The amplitudes of both grid–1 and gap voltages follow the preset amplitude ramp. As expected the trigger signal does not emerge.
Similar ramps where then used to provoke an electric arc. To this end the amplitude of the flat top of the amplitude ramp was set to 2 kV and the rise time to 1500 ms. Figure 7.7 displays the result.
Again the rise of both the grid–1 and the gap voltage can be seen. After about 110 ms the gap voltage collapses due to an electric arc. About 20 ms later also the grid–1 voltage collapses due to the current limiter of the tetrode. However, the trigger signal rises already before the electric arc occurs and therefore before the trigger condition is reached. Furthermore, the trigger signal rises for 100 ms only although the default hold time that is realized with a monostable flipflop (cf. chapter 5.2.2) is 1 s. This behavior could be reproduced for other acceleration cycles as well. Before the arc detector can be used with the control system this issue has to be solved.

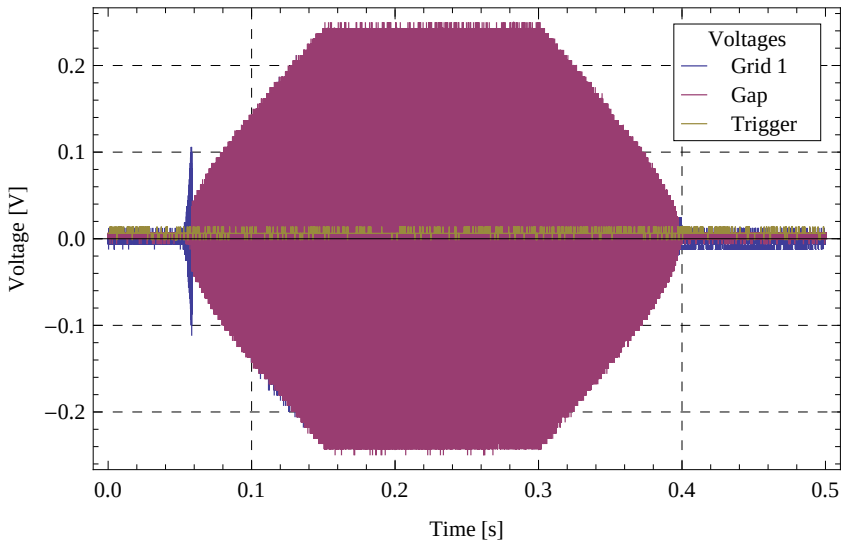

Figure 7.6: *Measurement of the trigger signal (divided by 5 for better visibility), the grid–1 voltage, and the gap voltage in a realistic acceleration cycle producing no electric arc.*

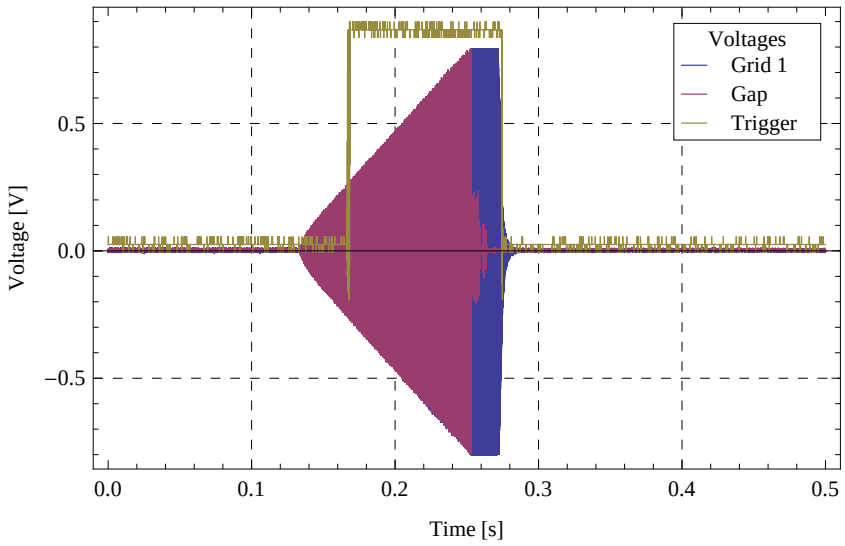

Figure 7.7: *Measurement of the trigger signal (divided by 5 for better visibility), the grid–1 voltage, and the gap voltage in a realistic acceleration cycle producing an electric arc.*

7.4 Error Analysis

For analyzing the failure of the setup in the case of a realistic ramp, the software tool TimeQuest Analyzer that is part of the development software Quartus was used. This analysis yielded a timing problem in two packages which is causing glitches on the trigger signal.
One was the divider used in the arc detector core. This devider was created with the MegaWizard Plug–In Manager, which is also a tool included in Quartus that accesses directly the original libraries of Quartus.
The second one was the Hilbert transformator, which is included in the amplitude and phase detector core. This package was adopted from the RF group's VHDL library.
Neither a change of the settings for the fitting and routing of the synthesis of the algorithm in Quartus to several optimizations, nor multicycling the respective signals had any effect on the timing problem. Synthesis is the process of transforming the VHDL code to a connection diagram that is implemented on the FPGA. The timing problem originates from the fact that signals in both packages mentioned are not available in time.
Both packages already worked without any problems in other projects. Furthermore about 75 % of the logic–cell rescources of the FGPA are in use, which is a high value because it involves a very complex routing. Is the routing too complex timing problems can occur. Due to these facts it is to assume that the designed algorithm including the detector framework and the arc detector core is too complex and extensive for being implemented on a Cyclone III FPGA.

Chapter 8

Summary and Future Prospects

In this thesis a configurable digital arc detector for ferrite–loaded cavities was developed, realized and tested. The method of arc detection is based on the comparison of a preset threshold with the ratio of the actual values of the grid–1 voltage and the gap voltage. The functionality was investigated in a test setup as well as in a SIS–18 prototype cavity.

The hardware chosen is a combination of an FPGA Interface Board and an ADC–DAC–FIB Adapter Board, which both were developed in the RF group at GSI and provide all required interfaces as well as field programmable gate arrays. As a first step the hardware of the FAB was reconfigured to meet the requirements of two RF input channels for signals of a maximal amplitude of 10 dBm.
In a next step an algorithm for arc detection was developed. Therefore the detector framework was designed and developed as a basis consisting of a part for the FIB as well as for the FAB. It provides the packages for the communication with all required I/O interfaces such as RS–232 and the internal communication via FUB. The detector framework stands out due to the possibility to realize diverse types of configurable detectors.
After its design and development including simulations, the arc detector core, which is the core piece of the arc detection algorithm, was implemented in the detector framework.
The configurability of the detector on a PC via RS–232 was realized by programming a configuration file for the program RFDevConf, which provides an user friendly graphical interface (cf. chapter 5.3). The final step in realizing the arc detector was the assembly within a RF housing for the operation in a 19–inch rack.

After the realization of the arc detector its functionality has been verified within a test setup. All requirements without any exception have been met. When applying the arc detector in a realistic setup involving a SIS–18 prototype cavity, it was shown that at a constant frequency the arc detector worked as expected. For realistic acceleration cycles using frequency and amplitude ramps glitches occurred on the trigger signal of the arc detector, which are caused by a timing problem of two packages within the algorithm originating from an insufficient synthesis.

One strategy is to include a PLL for generating the clock signal and for synchronizing the different clock domains. Another strategy is to use a clock with a lower frequency than 50 MHz. To this end several packages have to be reconfigured.

As already stated in chapter 7.4 the used algorithm for arc detection including the detector framework and the detector core is because of the extensive routing too complex for being implemented on a Cyclone III. One possibility is to optimize the code by reducing the bit width of some signals, so that the routing during the synthesis is less elaborate. Another possibility is to use an FPGA that provides more resources like the Arria II on the FAB III, which will be used in the future at the RF group.

Appendix A

Tables and Figures

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.99702	9.925	9.954
0.89378	8.890	9.946
0.56286	5.610	9.967
0.31537	3.143	9.966
0.14284	1.422	9.956
0.07128	0.716	10.045
0.03140	0.323	10.288
0.01570	0.167	10.638
0.01259	0.135	10.726
0.00785	0.089	11.339
0.00495	0.061	12.324
0.00311	0.045	14.464
0.00175	0.036	20.358
0.00126	0.034	27.013
0.00099	0.033	33.287
0.00079	0.032	40.551
0.00050	0.032	64.100
0.00036	0.032	89.791
0.00000	0.032	

Table A.1: *Measurement of input voltage, output voltage and the according ratio of channel ADC1 at 0.4 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
1.00268	9.660	9.634
0.89803	8.656	9.639
0.56710	5.460	9.628
0.31678	3.058	9.653
0.14284	1.385	9.697
0.07170	0.697	9.721
0.03140	0.315	10.033
0.01584	0.163	10.291
0.01259	0.132	10.487
0.00788	0.087	11.045
0.00495	0.060	12.041
0.00311	0.044	14.142
0.00177	0.036	20.138
0.00126	0.034	27.013
0.00099	0.032	32.187
0.00079	0.032	40.478
0.00050	0.032	64.100
0.00036	0.032	89.791
0.00000	0.032	

Table A.2: *Measurement of input voltage, output voltage and the according ratio of channel ADC1 at 1 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
1.00126	9.780	9.768
0.89661	8.765	9.776
0.56569	5.530	9.776
0.31537	3.095	9.814
0.14284	1.401	9.808
0.07156	0.706	9.866
0.03140	0.318	10.129
0.01570	0.165	10.511
0.01259	0.133	10.567
0.00786	0.088	11.192
0.00496	0.060	12.087
0.00311	0.044	14.271
0.00175	0.036	20.472
0.00126	0.034	27.013
0.00099	0.033	33.193
0.00079	0.033	41.818
0.00050	0.032	64.100
0.00036	0.032	89.791
0.00000	0.032	

Table A.3: *Measurement of input voltage, output voltage and the according ratio of channel ADC1 at 2 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.99843	10.060	10.076
0.89378	9.016	10.087
0.56569	5.690	10.059
0.31537	3.183	10.093
0.14284	1.441	10.089
0.07142	0.725	10.152
0.03140	0.327	10.415
0.01570	0.169	10.766
0.01259	0.137	10.885
0.00785	0.090	11.467
0.00496	0.062	12.410
0.00311	0.045	14.464
0.00175	0.036	20.529
0.00126	0.034	27.013
0.00099	0.033	33.287
0.00079	0.033	41.818
0.00050	0.032	64.100
0.00036	0.032	89.791
0.00000	0.032	

Table A.4: *Measurement of input voltage, output voltage and the according ratio of channel ADC1 at 3 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.99702	10.201	10.231
0.89237	9.140	10.242
0.56286	5.765	10.242
0.31396	3.226	10.275
0.14284	1.461	10.229
0.07142	0.735	10.292
0.03140	0.332	10.575
0.01570	0.171	10.893
0.01259	0.138	10.964
0.00785	0.091	11.594
0.00495	0.062	12.526
0.00311	0.045	14.464
0.00177	0.036	20.365
0.00126	0.034	27.013
0.00099	0.033	33.287
0.00079	0.033	41.818
0.00050	0.032	64.100
0.00036	0.032	89.791
0.00000	0.032	

Table A.5: *Measurement of input voltage, output voltage and the according ratio of channel ADC1 at 4 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
1.01116	10.270	10.157
0.90510	9.192	10.156
0.57134	5.798	10.148
0.31820	3.248	10.207
0.14425	1.469	10.184
0.07255	0.739	10.186
0.03182	0.334	10.497
0.01598	0.173	10.826
0.01273	0.139	10.921
0.00798	0.092	11.534
0.00503	0.062	12.315
0.00315	0.046	14.428
0.00178	0.036	20.203
0.00127	0.034	26.713
0.00101	0.033	32.681
0.00080	0.033	41.082
0.00050	0.032	64.100
0.00036	0.032	89.791
0.00000	0.032	

Table A.6: *Measurement of input voltage, output voltage and the according ratio of channel ADC1 at 5 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
1.00833	10.168	10.084
0.90227	9.104	10.090
0.56993	5.742	10.075
0.31678	3.213	10.143
0.14425	1.454	10.080
0.07227	0.732	10.129
0.03182	0.331	10.402
0.01598	0.171	10.700
0.01273	0.138	10.842
0.00796	0.091	11.429
0.00503	0.062	12.315
0.00315	0.045	14.396
0.00178	0.036	20.203
0.00127	0.034	26.713
0.00101	0.033	32.727
0.00080	0.033	41.082
0.00050	0.032	64.100
0.00036	0.032	89.791
0.00000	0.032	

Table A.7: *Measurement of input voltage, output voltage and the according ratio of channel ADC1 at 6 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.99702	9.885	10.014
0.89378	8.852	10.015
0.56286	5.585	9.998
0.31537	3.130	10.015
0.14284	1.422	10.055
0.07128	0.722	10.211
0.03140	0.338	10.913
0.01570	0.198	12.728
0.01259	0.176	14.174
0.00785	0.156	20.056
0.00495	0.150	27.109
0.00311	0.146	46.926
0.00175	0.145	82.024
0.00126	0.144	115.315
0.00099	0.144	145.254
0.00079	0.143	181.212
0.00050	0.144	287.637
0.00036	0.144	363.655
0.00000	0.144	

Table A.8: *Measurement of input voltage, output voltage and the according ratio of channel ADC2 at 0.4 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.99278	9.618	9.688
0.88954	8.615	9.685
0.56144	5.435	9.680
0.31396	3.045	9.699
0.14284	1.384	9.689
0.07099	0.703	9.902
0.03111	0.330	10.607
0.01570	0.194	12.358
0.01245	0.173	13.901
0.00781	0.155	19.855
0.00554	0.149	26.877
0.00311	0.146	46.926
0.00177	0.144	81.459
0.00125	0.144	114.925
0.00099	0.144	144.841
0.00079	0.144	181.503
0.00050	0.144	286.826
0.00036	0.144	399.307
0.00000	0.144	

Table A.9: *Measurement of input voltage, output voltage and the according ratio of channel ADC2 at 1 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.98995	9.735	9.834
0.88671	8.719	9.833
0.56003	5.500	9.821
0.31254	3.081	9.858
0.14142	1.400	9.899
0.07099	0.711	10.015
0.03111	0.333	10.703
0.01556	0.196	12.599
0.01245	0.174	13.941
0.00778	0.156	20.056
0.00553	0.150	27.091
0.00311	0.146	46.926
0.00175	0.144	82.116
0.00125	0.144	115.315
0.00099	0.144	145.254
0.00079	0.144	182.479
0.00050	0.144	288.451
0.00036	0.144	404.061
0.00000	0.144	

Table A.10: *Measurement of input voltage, output voltage and the according ratio of channel ADC2 at 2 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.98854	10.012	10.128
0.88530	8.970	10.132
0.55861	5.659	10.130
0.31254	3.169	10.139
0.14142	1.440	10.182
0.07071	0.730	10.324
0.03111	0.342	10.992
0.01556	0.199	12.792
0.01245	0.176	14.142
0.00778	0.157	20.185
0.00553	0.151	27.217
0.00311	0.146	46.926
0.00175	0.145	82.686
0.00125	0.144	115.315
0.00099	0.144	145.254
0.00079	0.144	182.479
0.00050	0.144	288.451
0.00036	0.144	400.879
0.00000	0.144	

Table A.11: *Measurement of input voltage, output voltage and the according ratio of channel ADC2 at 3 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.98712	10.148	10.280
0.88247	9.092	10.303
0.55861	5.736	10.268
0.31113	3.213	10.327
0.14142	1.459	10.317
0.07071	0.740	10.465
0.03097	0.346	11.172
0.01556	0.202	12.985
0.01245	0.178	14.303
0.00778	0.157	20.185
0.00553	0.151	27.217
0.00311	0.146	46.926
0.00175	0.145	82.686
0.00125	0.145	116.116
0.00099	0.144	145.254
0.00079	0.144	182.479
0.00050	0.144	288.451
0.00036	0.144	404.061
0.00000	0.144	

Table A.12: *Measurement of input voltage, output voltage and the according ratio of channel ADC2 at 4 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
1.00126	10.215	10.202
0.89661	9.140	10.194
0.56569	5.766	10.193
0.31537	3.233	10.251
0.14284	1.467	10.271
0.07071	0.744	10.522
0.03154	0.349	11.066
0.01584	0.202	12.753
0.01259	0.178	14.142
0.00789	0.157	19.895
0.00561	0.151	26.895
0.00315	0.146	46.295
0.00178	0.145	81.373
0.00127	0.144	113.389
0.00101	0.144	142.810
0.00080	0.144	179.267
0.00050	0.144	288.451
0.00036	0.144	404.061
0.00000	0.144	

Table A.13: *Measurement of input voltage, output voltage and the according ratio of channel ADC2 at 5 MHz. The respective last digit can be considered as error–prone.*

Input voltage [Vp]	Output voltage [V]	Ratio output to input voltage
0.99843	10.100	10.116
0.89378	9.039	10.113
0.56427	5.702	10.105
0.31396	3.195	10.177
0.14284	1.450	10.152
0.07156	0.735	10.271
0.03154	0.344	10.908
0.01584	0.200	12.627
0.01259	0.176	13.983
0.00788	0.156	19.804
0.00560	0.150	26.784
0.00315	0.146	46.295
0.00178	0.145	81.373
0.00127	0.144	113.515
0.00101	0.144	142.810
0.00080	0.144	179.267
0.00050	0.144	288.451
0.00036	0.144	404.061
0.00000	0.144	

Table A.14: *Measurement of input voltage, output voltage and the according ratio of channel ADC2 at 6 MHz. The respective last digit can be considered as error–prone.*

Set trigger threshold	Theoretical value of input voltage [Vp]	Actual value of input voltage [Vp]
0.9	0.891	0.938
0.8	0.792	0.832
0.7	0.693	0.723
0.6	0.594	0.625
0.5	0.495	0.519
0.4	0.396	0.414
0.3	0.297	0.311
0.2	0.198	0.209

Table A.15: *Measurement of actual trigger threshold at various set thresholds at an RF input signal for ADC1 channel of 1 MHz. The respective last digit can be considered as error–prone.*

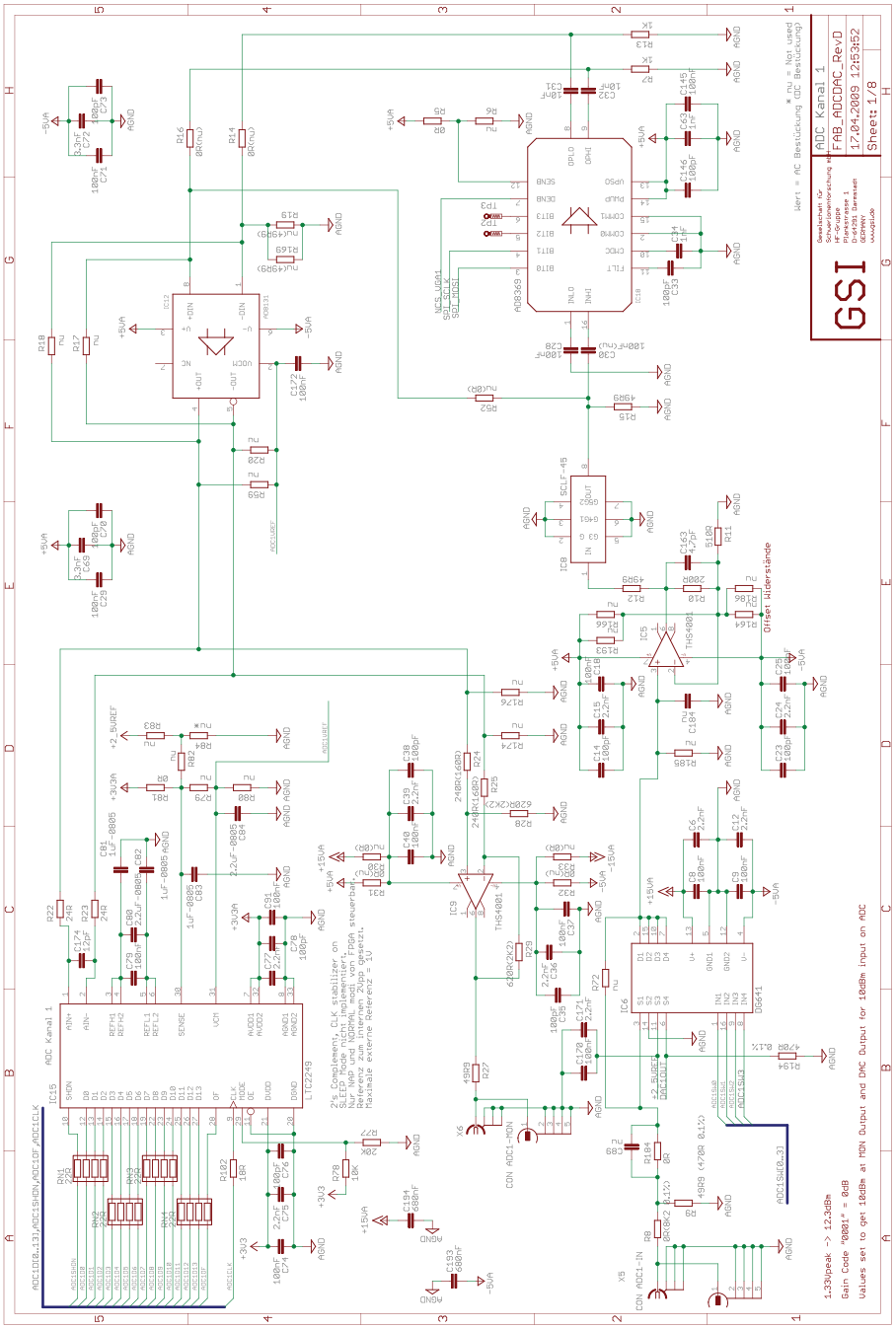

Figure A.1: *Circuit diagram of ADC–DAC–FAB. [22]*

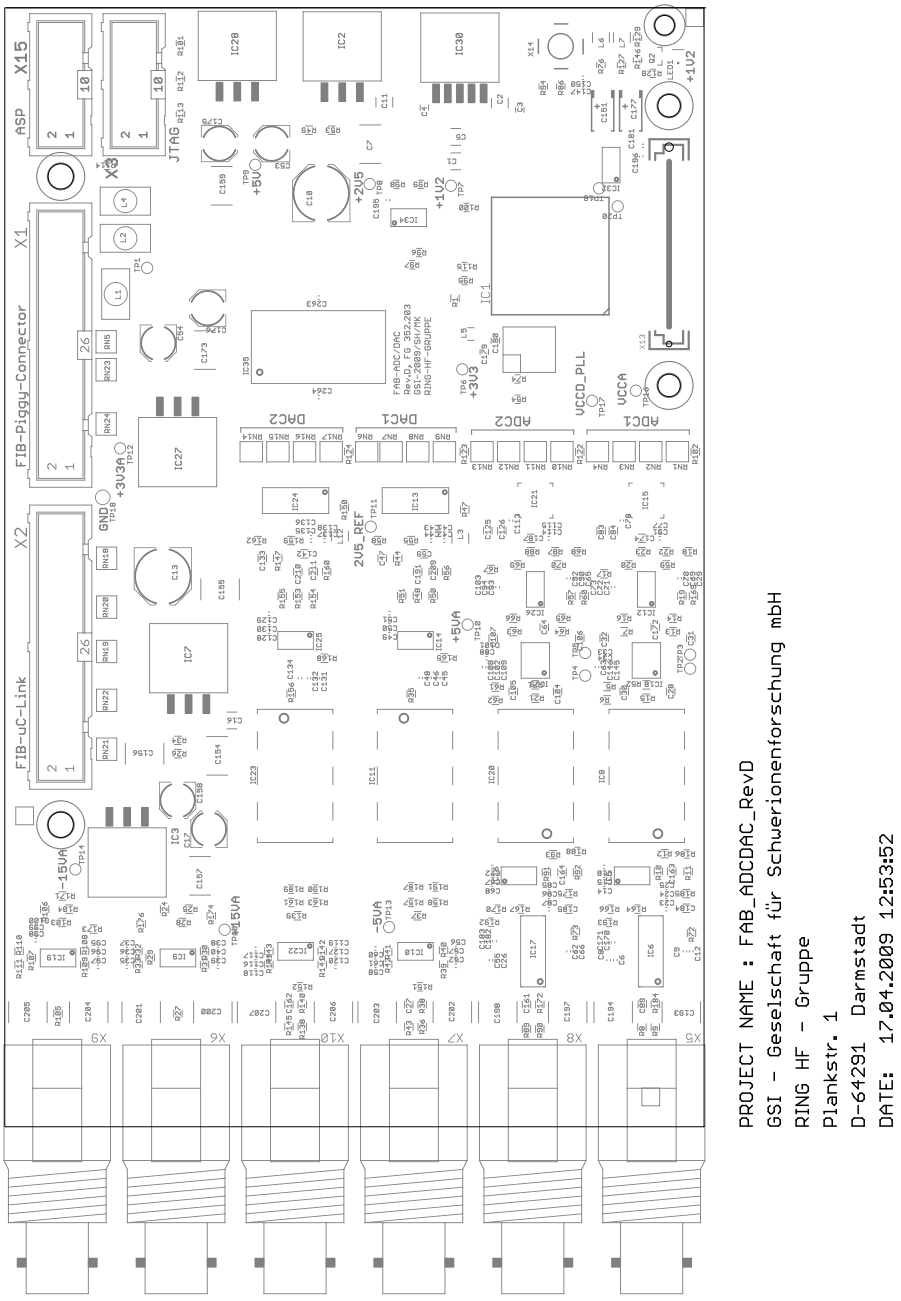

Figure A.2: *Top side assembly diagram of ADC–DAC–FAB. [23]*

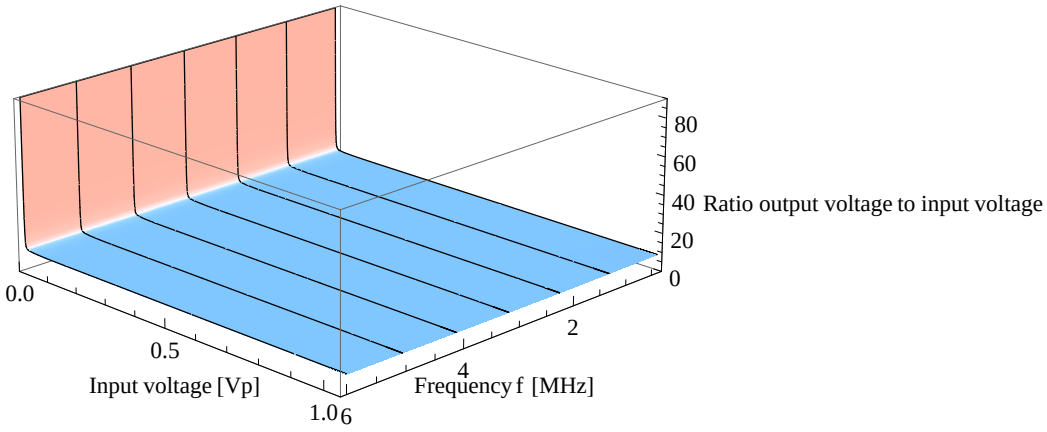

Figure A.3: *Input to output ratio of ADC1 channel: Plotted is ratio output voltage as a function of the input voltage and the frequency.*

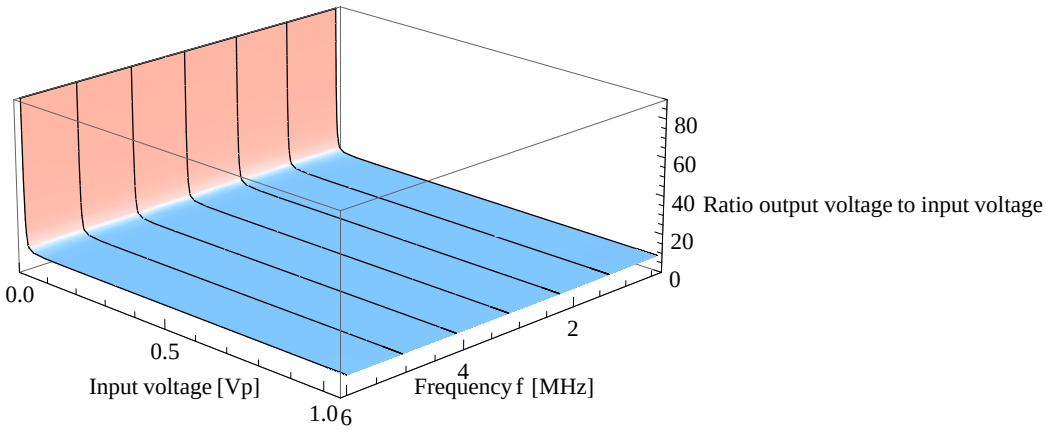

Figure A.4: *Input to output ratio of ADC2 channel: Plotted is ratio output voltage as a function of the input voltage and the frequency.*

Abbreviations

AC	Alternating Current
ADC	Analog–to–Digital Converter
ASP	Active Serial Programming
BNC	Bayonet Neill Concelman
cERL	compact Energy Recovery Linac
cf.	confirm
CORDIC	COordiante Rotation DIgital Computer
DAC	Digital–to–Analog Converter
DC	Direct Current
DDS	Direct Digital Synthesis
DSP	Digital Signal Processor
e.g.	exempli gratia FAB
FIB Adapter Board	
FAIR	Facility for Antiproton and Ion Research
FIB	FPGA Interface Board
FIR	Finite Impulse Response
FPGA	Field–Programmable Gate Array
FUB	FPGA Universal Bus
GSI	GSI Helmholtzzentrum für Schwerionenforschung (formerly Gesellschaft für Schwerionenforschung)
i.e.	it est
I/O	Input/Output
JTAG	Joint Test Action Group
KEK	kou enerugii kasokuki kenkyuukikou (=High Energy Accelerator Research Organization)
LAN	Local Area Network
LED	Light–emitting diode
LEMO	Léon Mouttet
μC	microcontroller
PC	Personal Computer
PLC	Programmable Logic Controller
PLL	Phase–Locked Loop
RAM	Random–Access Memory
RESR	Recycled Experimental Storage Ring
RF	Radio Frequency
RS–232	Recommended Standard 232

SIS 18	Schwerionen Synchrotron 18 (= heavy ion synchrotron, 18 stands for the rigidity of 18 Tm)
SIS 100	Schwerionen Synchrotron 100 (= heavy ion synchrotron, 100 stands for the rigidity of 100 Tm)
VGA	Variable–Gain Amplifier
VHDL	Very High Speed Integrated Circuit Hardware Description Language

Symbols

a	Constant, Radius of a cavity
A	Gas constant of Paschen's law
A_n	Factor after n rotations
B	Gas constant of Paschen's law
B_Θ	Θ component of magnetic field
β	Velocity in terms of the speed of light
c	Speed of light
C_{Total}	Capacity of a cavity
d	Distance
$\delta()$	Delta function
ΔW	Energy gain of a particle
E	Electric field
E_z	z component of an electric field
$f()$	Function
$\hat{f}()$	Function in frequency domain
f_r	Resonance frequency
$F\{\}$	Fourier transform
ϕ	Arbitrary rotation angle
ϕ_i	Arbitrary rotation angle for step i
Φ_s	Phase of a synchronous particle
$g()$	Function
$\hat{g}()$	Function in frequency domain
$g[]$	Sequence
γ	Lorentz factor
h	Integer
$h[]$	Impulse response
$H\{\}$	Hilbert transform
i	Integer
J_0	Bessel function of zero order
k	Integer
K	Constant
k_{lim}	Scalable threshold for trigger condition
l	Length of a cavity
$L(\mu_r)$	Impedance depending on magnetic permeability
λ_{RF}	Wavelength of a radio frequency wave
m	Rest mass of a particle
ω	Frequency

ω_s	Synchrotron frequency
p	Pressure
q	Charge of an particle
Q	Quality factor of a cavity
r	Radius
S_i	Sign of ith rotation of the CORDIC algorithm
t	Variable
T	Transit time factor
τ	Variable
τ_{drop}	Decay time
U_{g1}	Actual grid–1 voltage
$U_{g1,n}$	Nominal grid–1 voltage
U_{gap}	Actual gap voltage
$U_{gap,n}$	Nominal gap voltage
v	Velocity
V_0	Voltage amplitude
V_B	Breakdown voltage
W_s	Energy of a synchronous particle
x	x component of a vector in the CORDIC algorithm
x'	x component of a vector after rotation in the CORDIC algorithm
x_i	x component of a vector after i rotations in the CORDIC algorithm
x_n	x component of a vector after n rotations in the CORDIC algorithm
x_{i+1}	x component of a vector after $i+1$ rotations in the CORDIC algorithm
y	y component of a vector in the CORDIC algorithm
y'	y component of a vector after rotation in the CORDIC algorithm
y_i	y component of a vector after i rotations in the CORDIC algorithm
y_n	y component of a vector after n rotations in the CORDIC algorithm
y_{i+1}	y component of a vector after $i+1$ rotations in the CORDIC algorithm

List of Figures

List of Tables

Bibliography

[1] K. Wille, *Physik der Teilchenbeschleuniger und Synchrotronstrahlungsquellen*, Teubner Studienbücher, Stuttgart (1996)

[2] O. Boine–Frankenheim, *Introduction to Accelerator Physics*, lecture notes, GSI, Darmstadt (2010)

[3] O. Boine–Frankenheim, *Introduction to Accelerator Physics*, presentation slides, GSI, Darmstadt (2010)

[4] F. Emery et al., *System and method for arc detection in dynamoelectric machines*, U.S. patent 4771355, Electric Power Research Institute, Palo Alto (September 1988)

[5] J. Zuercher et al., *Arc detection using current variation*, U.S. patent 5561605, Eaton Corporation, Cleveland (October 1996)

[6] C. Tennies et al., *Timing Window Arc Detection*, U.S. patent 5208542, Eaton Corporation, Cleveland (May 1993)

[7] S. Schäfer, H.G. König, *Überschlagserkennung an Kavitäten (Version 1.7)*, GSI, Darmstadt (April 2008)

[8] T. Miura et al., *Low–Level RF System for cERL*, Proceedings of IPAC'10, Kyoto, KEK, Tsukuba (May 2010)

[9] Analog Devices Inc., *LF-2.7 GHz RF/IF Gain and Phase Detector – AD8302 Datasheet*, Analog Devices Inc., Norwood (2002)

[10] M. Omet, *Development, Construction and Test of a Radiofrequency Amplitude Detector for the Recycled Experimental Storage Ring RESR at the Facility for Antiproton and Ion Research FAIR,* Bachelor–Thesis, TU Darmstadt/GSI, Darmstadt (2009)

[11] S. Schäfer, J. Gao and C. Steger, *Modeling of Accelerating Cavities in the MHz-range loaded with magnetic Material*, presentation slides, TU Darmstadt, Darmstadt (2009)

[12] T. Wollmann, *Entwurf und Implementierung eines digitalen Phasen- und Amplitudendetektors für eine HF-Beschleunigerkaviät*, Diplomarbeit, Technische Univerität Darmstadt / GSI, Darmstadt (September 2009)

[13] U. Fischer, *Entwurf und Implementierung eines echtzeitfähigen Network–on–Chip für den Einsatz in zeitkritischen Regelungsaufgaben*,Projektbericht , Fachhochschule Fulda, Fulda (January 2005)

[14] M. Johansson, *The Hilbert transform*, Växjö University, Växjö (1999) http://www.fuchs-braun.com/media/d9140c7b3d5004fbffff8007fffffff0.pdf

[15] M. Penz, *The Hilbert–Transformation (in a nutshell),* blue sheet, Universität Innsbruck, Innsbruck (2010)

[16] U. Naundorf, *Digitale Elektronik: Theoretische Grundlagen und Schaltungsanalysen*, Oldenbourg Wissenschaftsverlag GmbH, München (2004)

[17] R. Andraka, *A survey of CORDIC algorithms for FPGA based computers*, Andraka Consulting Group Inc., North Kingstown (1998)

[18] S. Schäfer, *Workshop – Kleine Einführung in VHDL*, presentation slides, GSI, Darmstadt (2010), unpublished

[19] M. Kumm, *milramp*, private communication, GSI, Darmstadt (2011), unpublished

[20] R. Hartmann, *Interface–Karte für die Netzgeräte–Backplane und den Modulbus*, manual, GSI, Darmstadt (2009)

[21] K.–P. Ningel, *AWGRampGen*, private communication, GSI, Darmstadt (2011), unpublished

[22] M. S. Sanjari, *Schaltplan_FAB_ADCDAC_RevD.pdf*, GSI, Darmstadt (April 2009)

[23] M. S. Sanjari, *Bestueckung_TOP_FAB_ADCDAC_RevD.pdf*, GSI, Darmstadt (April 2009)

Acknowledgment

I would like to thank everyone who supported me writing this thesis starting with my supervisor Dipl.–Ing. (FH) Stefan Schäfer and my consultant Prof. Dr. Joachim Enders. Furthermore I thank Dr. Ulrich Laier, Dr. Klaus–Peter Ningel, Peter Moritz, Dr. Hans Günter König, Dr. Bernhard Zipfel, Thomas Winnefeld, Dr.-Ing. Harald Klingbeil, and Oliver Bitterling as well as Ibrahim Nsangou.
Beside this I would like to thank my family, in particular Marc Wengenroth, and my friends for the great support.

Mathieu Omet

Declaration – Erklärung

I declare that I wrote this master–thesis independently and without any other references and resources than stated in the bibliography.

Hiermit erkläre ich, dass ich die vorliegende Master–Thesis selbstständig verfasst habe und keine als die angegebenen Referenzen und Hilfsmittel verwendet habe.

Darmstadt, August 2011