Development and Test of Klystron Linearization Packages for FPGA–based Low Level RF Control Systems of ILC–like Electron Accelerators

M. Omet*, *SOKENDAI, Hayama, Japan*
S. Michizono, T. Matsumoto, T. Miura, F. Qiu, *KEK/SOKENDAI, Tsukuba, Japan*
H. Schlarb, J. Branlard, *DESY, Hamburg, Germany*
W. Cichalewski, *TUL, Lodz, Poland*
B. Chase, P. Varghese, *FNAL, Batavia, USA*

***Abstract*—We report the development and implementation of two FPGA–based predistortion–type klystron linearization algorithms at the Fermi National Accelerator Laboratory (FNAL), USA and the Deutsches Elektronen Synchrotron (DESY), Germany. With those the generation of correction factors on the FPGA was improved, avoiding quantization and decreasing memory requirements. At FNAL the linearization algorithm was tested at the Advanced Superconducting Test Accelerator (ASTA) demonstrating a successful implementation. The functionality of the algorithm implemented at DESY was demonstrated successfully in a simulation.**

***Index Terms*—Amplifier, klystron, linearization, FPGA, ILC.**

I. Introduction

AT the International Linear Collider (ILC) [1] the superconducting cavities of the main linacs will be controlled using digital low level radio frequency (LLRF) techniques [2]. Figure 1 shows a schmematic of a typical LLRF control loop. The from the cavity picked up radio frequency (RF) is down converted in frequency by mixing with the local oscillator (LO) signal. The resulting signal, the intermediate frequency (IF), is digitized using a analog–to–digital converter (ADC). The digital signal is processed on an FPGA, which contains beside others the controller. The processed signal is converted from digital to analog. The analog signal is fed beside an RF signal to an IQ modulator for up conversion in frequency. The resulting RF signal is amplified by a klystron, which drives the cavity. In case of ILC groups of 39 cavities will be driven by single 10 MW multi–beam klystrons.

Typically the input–to–output characteristics of a klystron in both amplitude and phase are not linear. A schematic of a typical input–to–output characteristic is shown in Figure 2 in black. In order to operate the klystrons at ILC most cost effectively, it is intended to operate them 3% below the point of saturation. Since the feedback gain is proportional to the slope of the output amplitude, it converts to 0 in this region. In order to keep the feedback effective, it is required to keep the amplitude slope constant and the phase rotation at 0° until the point of saturation. The desired klystron output is shown in Figure 2 in red. This can be accomplished by using a klystron linearization. The linearization algorithms described in the following are predistortion–type linearizations, implemented in the firmware of the field programmable gate array (FPGA), on which beside others the digital LLRF controller is located. The predistortion characteristics are inverse to the non–linear characteristics of the klystron. The predistorer is typically located after the controller and the addition of feedforward tables and before transmitting the signals to the digital–to–analog converters (DACs). The predistortion is typically generated in dependency of the signal amplitude.

* momet@post.kek.jp

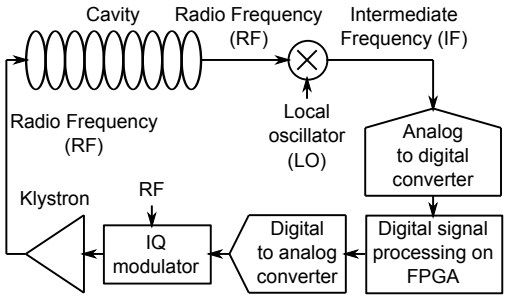

Fig. 1. Schematic of a typical digital LLRF control loop.

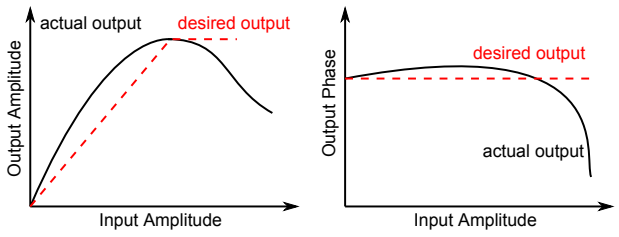

Fig. 2. Schematic of the klystron amplitude and phase output characteristics.

In the past linearization concepts were already implemented based on analog circuits [3]. The over the recent years improved capabilities of FPGAs allowed not only the implementation of digital LLRF feedback controllers but also the implementation of klystron linearization algorithms with high effectiveness and flexibility [4]. Two algorithms implemented on FPGAs of two different manufacturers are described and compared in the following.

II. Klystron Linearization Implemented at DESY

At DESY the Free Electron Laser in Hamburg (FLASH) [5] is operated, which uses the same superconducting TESLA–type 9–cell cavity technology [6] as will be used at ILC. The digital LLRF control system at FLASH was based on the VME standard, before it was upgraded to μTCA.4 [7]. For the VME system a predistortion–type squared amplitude dependent direct lookup table–based klystron linearization was implemented (see [4]), which allowed a complex correction as shown in equation (1).

$$\begin{pmatrix} I' \\ Q' \end{pmatrix} = \begin{pmatrix} f_i(A^2) & -f_q(A^2) \\ f_q(A^2) & f_i(A^2) \end{pmatrix} \begin{pmatrix} I \\ Q \end{pmatrix} \quad , \tag{1}$$

where I and Q is the input of the linearization algorithm, $f_i(A^2)$ and $f_q(A^2)$ are the correction factors, and I' and Q' is the output of the algorithm.

As part of the presented study this concept was reintroduced for the μTCA.4–based LLRF control system. The target device for the implementation of the algorithm was a Xilinx Kintex 7 (K355/K420) FPGA on the LLRF controller card (uTC). The firmware creation tool set covered Notepad ++, ISE Design Suite 14.4, and ISim. The schematic of the implemented VHDL package is shown in Figure 3. From the algorithm input I and Q (18 bit each) the squared amplitude is computed. The squared amplitude is truncated to 12 bit and used as an address for two lookup tables. These contain correction factors, which are applied to the input I and Q values by a complex multiplication, resulting in the output values I' and Q' (18 bit each). Since the address range is 12 bit and the processed signals have a width of 18 bit, a quantization error of 6 bits occurs.

III. Klystron Linearization Implemented at FNAL

At FNAL ASTA [8] is under construction. Since it is beside an user machine also an ILC R&D accelerator, the digital LLRF control system was designed with ILC in mind.

As part of the presented study a predistortion–type amplitude dependent klystron linearization algorithms was implemented and tested. The target hardware was an Altera Cyclone II FPGA on the multi–cavity field control (MFC) module [9]. The tools used for the manipulation and creation of the FPGA firmware were Matlab 2012b, Simulink 2012b, DSP Builder 13.0, ModelSim, and Quartus II 13.0. The algorithm implemented was designed for the linearization of the amplitude only. Its principle is based on equation (2).

$$\begin{pmatrix} I_{out} \\ Q_{out} \end{pmatrix} = f_{corr}(A) \begin{pmatrix} I_{in} \\ Q_{in} \end{pmatrix} \quad , \tag{2}$$

where, I_{in} and Q_{in} is the algorithm input, $f_{corr}(A)$ a 3rd order polynomial function depending on A, and I_{out} and Q_{out} is the algorithm output. A is the amplitude of I_{in} and Q_{in}. Figure 4 shows a schematic of the linearization algorithm. From the I_{in} and Q_{in} values the amplitude is computed and by a 3rd order polynomial function a correction factor is calculated. Furthermore an amplitude limitation is included, which compares the expected output amplitude to a preset limit. If the limit is exceeded, the correction factor is set to $f_{corr} = \frac{limit}{A}$. By two switches the linearized or the original I_{in} and Q_{in} values can be chosen as the output of the algorithm.

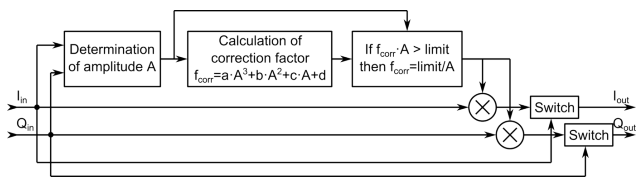

Fig. 4. Schematic of third order polynomal–based klystron linearization algorithm.

IV. Test and Comparison of Algorithms

In Table I the clock cycles required for the application of the linearization algorithms are compared. This includes the calculation of the squared amplitude or amplitude, respectively, as well as the generation of the correction factor(s). Beside this the loop delays added due to the implementation of the algorithms are listed.

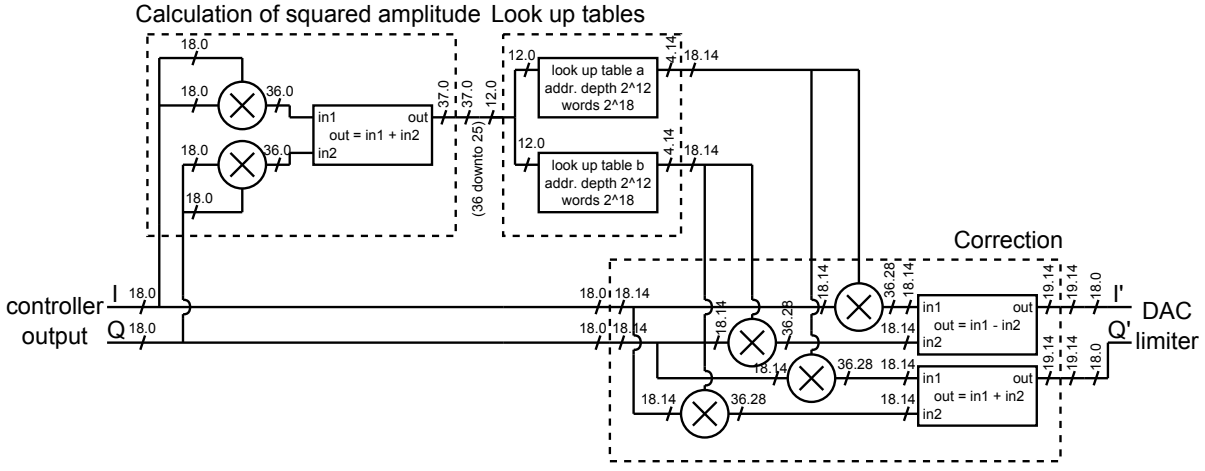

Fig. 3. Schematic of the direct lookup table–based klystron linearization package for the μTCA.4–based LLRF control sytsem at DESY.

TABLE I
COMPARISON OF DELAYS. (* INCLUDING AMPLITUDE LIMITER)

Algorithm	Correction factor generation [clk. cyc.]	Added loop delay [clk. cyc.]
Direct LUT	6	2
3rd order	31*	1

The algorithm with the shortest computation time of the correction factors is the one based on direct lookup tables. It requires about 0.08 μs. The computation by the 3rd order polynomial requires about 0.5 μs. It should be noted that the clock frequencies are different, namely 81.25 MHz for the Kintex 7 and 62.5 MHz for the Cyclone II. If the application allows quantization errors, the lookup table–based method is preferable. In the case quantization has to be avoided and amplitude linearization only is sufficient, the 3rd polynomial–based klystron linearization algorithm is the method of choice. In both cases the computation time is short enough for the linearization of a klystron driving a superconducting cavity. During the RF pulse the klystron working point typically does not change drastically. Furthermore the cavity response is sufficiently slow compared to the computation time, due to the cavity's high loaded quality factor.

From the viewpoint of total added loop delay, the 3rd order polynomial function-based algorithm with only 1 clock cycle added is the best. This is due to the fact, that in the linearization algorithm also the amplitude limitation is included. The direct lookup table–based algorithm adds 2 clock cycles of loop delay. In the case it is combined with an amplitude limiter the delay increases to 3 clock cycles. In both cases the added loop delay is negligible small compared to the typical total loop of 1 to 2 μs.

The functionality of the direct lookup table–based linearization algorithm implemented at DESY could only be verified in a iSim simulation. To this end a non–linear klystron characteristic in amplitude and phase recorded at the 10 MW klystron of FLASH (ACC67) as shown in Figure 5 in blue was implemented in a VHDL test bench. Furthermore a MATLAB script for the calculation of the lookup table content was written. The result of the simulation of the linearization is shown in Figure 5 in purple. The amplitude was linearized sufficiently. The output phase stayed constant except a slight fluctuation at high input amplitudes. With this a proof of concept was demonstrated.

The 3rd order polynomal–based klystron linearization algorithm implemented at FNAL was tested at ASTA. To this end the 5 MW klystron (Thales TH2104C) controlled by the MFC board, including the FPGA–based controller and linearization algorithm, was run into a water load, as shown in the schematic Figure 6.

By a klystron input amplitude scan in feedforward (FF) or open loop only operation, the klystron input–to–output amplitude characteristic was obtained. Based on this the factors a, b, c, and d of the 3rd order polynomial function were determined. Furthermore a limit value corresponding to the point of saturation was set. After the activation of

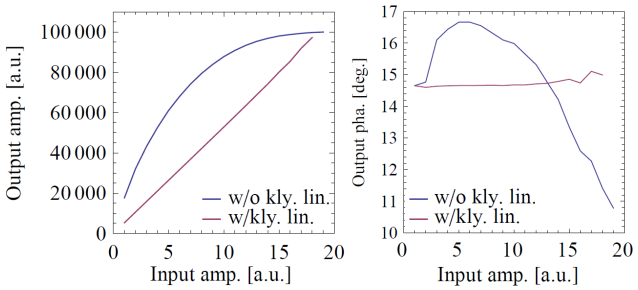

Fig. 5. *Plots of result of iSim simulation without the klystron linearization (blue) and with linearization (purple). Left: Klystron linearization algorithm output amplitude [a.u.] versus input amplitude [a.u.]. Right: Klystron linearization algorithm output phase [°] versus input amplitude [a.u.].*

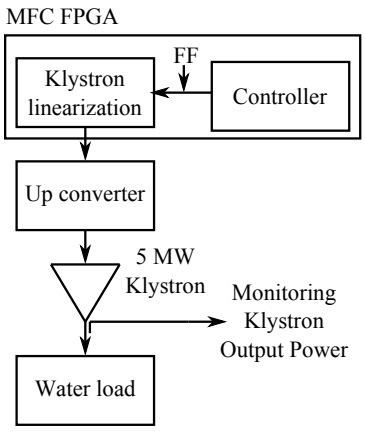

Fig. 6. *Schematic of the test setup at ASTA for the 3rd order polynomial–based klystron linearization algorithm. The 5 MW klystron is controlled by the MFC board and run into a water load.*

the klystron linearization a second klystron input amplitude scan was performed. Figure 7 shows the measured klystron output amplitude [sqrt(kW)] versus the input amplitude [a.u.] represented by blue dots. This characteristics agrees very well (less than 1% in average) with the expected output represented by the green graph in Figure 7. Also the limitation at the point at saturation is effective. By this a successful implementation of the algorithm was demonstrated.

V. CONCLUSION

In an international collaboration with DESY and FNAL two FPGA–based predistortion–type klystron linearization algorithms were implemented and tested. At DESY a direct lookup table–based algorithm was implemented in the scope of the new μTCA.4 hardware used for LLRF control at FLASH. The implementation was tested successfully in an iSim simulation.

At FNAL a linearization algorithm based on a 3rd order polynomial function was implemented. By this the quantization of the output of the linearization algorithm was avoided. Beside this the memory requirements could be reduced drastically, since only four factors had to be stored instead of two 12 bit lookup tables. Furthermore the total loop delay added could be reduced by 2/3 compared to the lookup table–based algorithm, since the amplitude limiter is already included. The

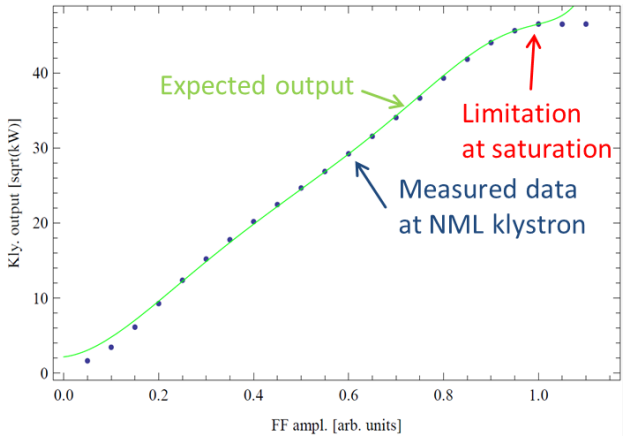

Fig. 7. *Klystron output amplitude [sqrt(kW)] versus FF amplitude [a.u.]: expected output (green), with 3rd order polynomial function–based linearization (blue).*

algorithm was successfully tested at a 5 MW klystron at FNAL ASTA. The measured klystron output characteristic agreed with an error of less that 1% in average with the predicted output.

REFERENCES

[1] http://www.linearcollider.org
[2] "The International Linear Collider – Technical Design Report", CERN, FNAL, KEK (2013).
[3] J. Yi, "Analog Predistortion Linearizer for High-Power RF Amplifiers", IEEE Transactions on Microwave Theory and Techniques, Vol. 48, No. 20 (2000).
[4] W. Cichalewski, "Linearization of Microwave High Power Amplifiers Chain in the RF Systems of Linear Accelerators for FLASH and X-FEL" (PhD Thesis), Technical University of Lodz, Lodz (2008).
[5] R. Kammering, "Feedbacks and Automation at the Free Electron Laser in Hamburg (FLASH)", THPPC121, Proceedings of ICALEPCS2013, San Francisco (2013).
[6] "TESLA Technical Design Report - PART II - The Accelerator ", http://flash.desy.de
[7] J. Branlard , "Status Update of the uTCA LLRF System for XFEL and FLASH Upgrade" (Presentation), ILC 9mA Meeting (2011).
[8] http://asta.fnal.gov/
[9] P. Varghese, "Multi–cavity Field Control (MFC) Module Description" (http://beamdocs.fnal.gov/AD/DocDB/0036/003676/001/MFC_Description.pdf), FNAL, Batavia (2009).